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Alan H. Blankenheimer (SBN 218713)
ablankenheimer@cov.com
Jo Dale Carothers (SBN 228703)
jcarothers@cov.com
Lesli Gallagher (SBN 250355)
lgallagher@cov.com
COVINGTON & BURLING LLP
9191 Towne Centre Drive, Suite 600
San Diego, CA 92122
Telephone: (858) 678-1800
Facsimile: (858) 678-1600

Attorneys for Plaintiff
Silicon Storage Technology, Inc.

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RICHARD W. WIEKING
CLERK, U.S. DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN JOSE

E-filing

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SILICON STORAGE TECHNOLOGY, INC.,

Plaintiff,

v.

TELEFUNKEN SEMICONDUCTORS AMERICA LLC & TELEFUNKEN SEMICONDUCTORS INTERNATIONAL LLC,

Defendants.

Case No. CV 12 6040 JCS

COMPLAINT FOR PATENT INFRINGEMENT

DEMAND FOR JURY TRIAL

Silicon Storage Technology, Inc. hereby alleges for its complaint against Telefunken Semiconductors America LLC and Telefunken Semiconductors International LLC, on personal knowledge as to its own activities and on information and belief as to the activities of others, as follows:

THE PARTIES

1. Silicon Storage Technology, Inc. ("SST") is a corporation organized and existing under the laws of the State of California, with its principal place of business at 450 Holger Way, San Jose, CA 95134. SST designs, manufactures and markets a diversified range of memory and non-memory products.

2. On information and belief, Defendant Telefunken Semiconductors America LLC is a corporation organized under the laws of the State of Delaware with its principal place of

business at 7501 Foothills Blvd., Roseville, CA 95747, and regularly conducts business in the Northern District of California.

3. On information and belief, Defendant Telefunken Semiconductors International LLC is a corporation organized under the laws of the State of Delaware with its principal place of business at 7501 Foothills Blvd., Roseville, CA 95747, and regularly conducts business in the Northern District of California.

4. On information and belief, Defendant Telefunken Semiconductors International LLC is the parent corporation of Defendant Telefunken Semiconductors America LLC.

NATURE OF THE ACTION

5. This is an action alleging infringement by Telefunken Semiconductors America LLC and Telefunken Semiconductors International LLC (collectively, "Telefunken") of United States Patent Nos. 6,593,177 and 6,743,674.

6. SST is the assignee of United States Patent No. 6,593,177 ("the '177 Patent"), entitled "Self Aligned Method of Forming a Semiconductor Memory Array of Floating Gate Memory Cells, and a Memory Array Made Thereby," issued on July 15, 2003. SST is owner of all rights, title and interest in and to this patent, including the right to recover for infringement. A true and correct copy of the '177 patent is attached hereto as Exhibit A.

7. SST is the assignee of United States Patent No. 6,743,674 ("the '674 Patent"), entitled "Method of Forming a Semiconductor Array of Floating Gate Memory Cells and Strap Regions, and a Memory Array and Strap Regions Made Thereby," issued on July 1, 2004. SST is owner of all rights, title and interest in and to this patent, including the right to recover for infringement. A true and correct copy of the '674 patent is attached hereto as Exhibit B.

JURISDICTION AND VENUE

8. This is an action for patent infringement arising under the patent laws of the United States. Title 35 U.S.C. §§ 271, et seq. This Court has subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338(a), because this action arises under the patent laws of the United States, including, but not limited to, 35 U.S.C. §§ 271, 281, 284, 285.

9. On information and belief, Telefunken conducts business in this district and as a result of this business has continuous and systematic contacts with this district including, but not limited to selling products in the Northern District of California.

10. In addition, SST has its principal place of business in the Northern District of California and the development of the technology at issue took place, at least in part, in the Northern District of California.

11. Venue is proper in this Court pursuant to 28 U.S.C. §§ 1391(b)-(c) and/or § 1400(b) because, *inter alia*, a substantial part of the events giving rise to the claims occurred in this district and because Telefunken is subject to personal jurisdiction in this district.

INTRA-DISTRICT ASSIGNMENT

12. Pursuant to Civil Local Rules 3-2(c) and 3-5, this is an Intellectual Property Action to be assigned on a district-wide basis.

BACKGROUND

13. SST has long been an industry-leading developer of Flash Memory technology, including process technology used to manufacture Flash Memory devices.

14. SST maintains an extensive patent portfolio based on its proprietary Flash Memory devices and processes.

15. On information and belief, Telefunken now operates a facility in Roseville, California at which Telefunken manufactures products using SST's proprietary SF5-18 technology.

16. Telefunken does not have a license to any SST patents or technology.

FIRST CAUSE OF ACTION:

INFRINGEMENT OF U.S. PATENT NO. 6,593,177

17. SST realleges and incorporates the allegations of Paragraphs 1-16 as if set forth herein in their entirety.

18. SST is informed and believes and thereon alleges that Telefunken has been and is now infringing the '177 Patent by making, using, selling and/or offering for sale in and/or

importing into the United States without authority products, including, without limitation, products manufactured using SST's SF5-18 technology at its Roseville facility.

19. By reason of Telefunken's acts alleged herein, SST has suffered damage in an amount to be proved at trial.

20. On information and belief, Telefunken threatens to continue to do the acts complained herein, and unless restrained and enjoined will continue to do so, all to SST's irreparable damage. It would be difficult to ascertain the amount of compensation which would afford SST adequate relief for such future and continuing acts. SST does not have an adequate remedy at law to compensate it for injuries threatened.

SECOND CAUSE OF ACTION:

INFRINGEMENT OF U.S. PATENT NO. 6,743,674

21. SST realleges and incorporates the allegations of Paragraphs 1-20 as if set forth herein in their entirety.

22. SST is informed and believes and thereon alleges that Telefunken has been and is now infringing the '674 Patent by making, using, selling and/or offering for sale in and/or importing into the United States without authority products, including, without limitation, products manufactured using SST's SF5-18 technology at its Roseville facility using SST technology.

23. By reason of Telefunken's acts alleged herein, SST has suffered damage in an amount to be proved at trial.

24. On information and belief, Telefunken threatens to continue to do the acts complained herein, and unless restrained and enjoined will continue to do so, all to SST's irreparable damage. It would be difficult to ascertain the amount of compensation which would afford SST adequate relief for such future and continuing acts. SST does not have an adequate remedy at law to compensate it for injuries threatened.

DEMAND FOR JURY TRIAL

25. SST demands a jury trial on all claims and issues so triable.

PRAYER FOR RELIEF

WHEREFORE, SST prays for an Order and entry of Judgment against Telefunken as follows:

A. For judgment that Telefunken has infringed and continues to infringe the '177 Patent;

B. For a preliminary and permanent injunction prohibiting Telefunken, and all persons or entities acting in concert with Telefunken, from infringing the '177 Patent;

C. For judgment that Telefunken has infringed and continues to infringe the '674 Patent;

D. For a preliminary and permanent injunction prohibiting Telefunken, and all persons or entities acting in concert with Telefunken, from infringing the '674 Patent;

E. For an award to SST of all damages resulting from the infringement of the '177 Patent and the '674 Patent, together with pre-judgment and post-judgment interest;

F. For the Court to declare this case exceptional under 35 U.S.C. § 285 and to award SST its reasonable attorneys' fees in this action;

G. For an award to SST of all costs and expenses of this action; and

H. For such other and further relief as this Court deems proper and just.

DATED this 28th day of November, 2012.

By: /s/ Jo Dale Carothers

Alan H. Blankenheimer
Jo Dale Carothers
Lesli Rawles Gallagher
COVINGTON & BURLING LLP
9191 Towne Centre Drive, Suite 600
San Diego, CA 92122
Telephone: (858) 678-1800
Facsimile: (858) 678-1600

Attorneys for Plaintiff
Silicon Storage Technology, Inc.

EXHIBIT A

US006593177B2

(12) **United States Patent**
Lee

(10) **Patent No.: US 6,593,177 B2**
(45) **Date of Patent: Jul. 15, 2003**

(54) **SELF ALIGNED METHOD OF FORMING A SEMICONDUCTOR MEMORY ARRAY OF FLOATING GATE MEMORY CELLS, AND A MEMORY ARRAY MADE THEREBY**

(75) Inventor: **Dana Lee**, Santa Clara, CA (US)

(73) Assignee: **Silicon Storage Technology, Inc.**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 4 days.

(21) Appl. No.: **09/972,179**

(22) Filed: **Oct. 5, 2001**

(65) **Prior Publication Data**

US 2002/0011608 A1 Jan. 31, 2002

Related U.S. Application Data

(63) Continuation of application No. 09/401,173, filed on Sep. 22, 1999, now Pat. No. 6,329,685.

(51) **Int. Cl.**[7] **H01L 29/64**

(52) **U.S. Cl.** **438/201**; 438/211; 438/257; 438/694

(58) **Field of Search** 438/201, 211, 438/257, 694, 314, 315

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,103,573 A * 8/2000 Harari et al. 438/257

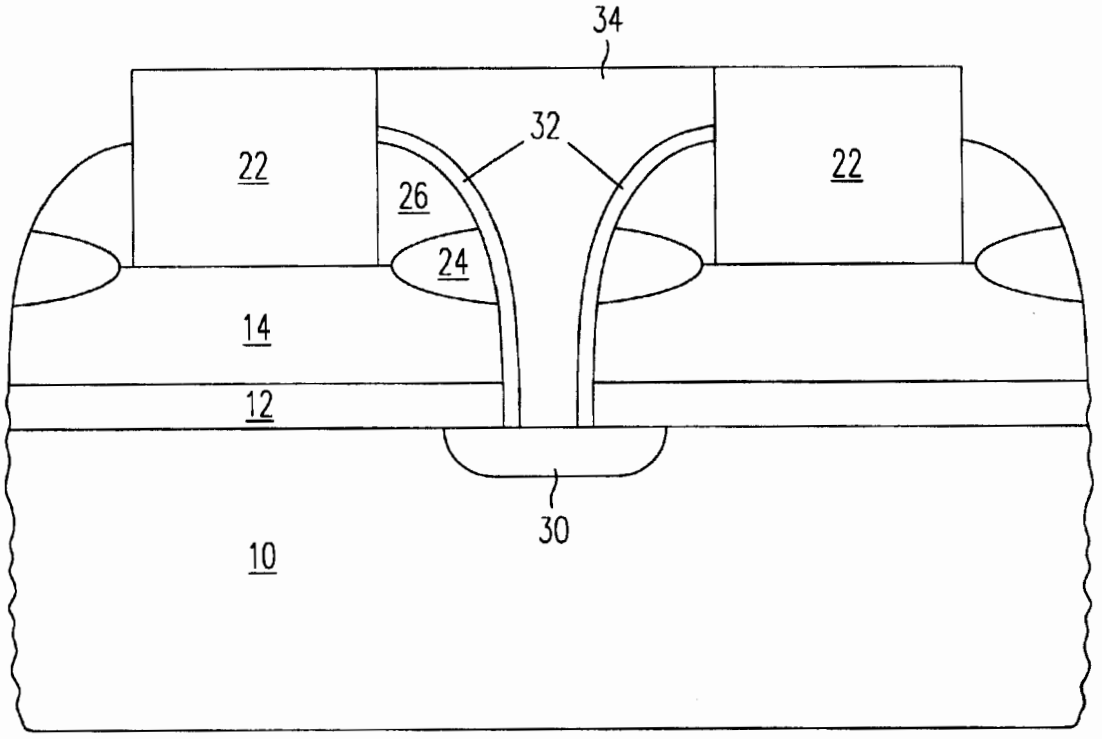
* cited by examiner

Primary Examiner—Edward Wojciechowicz
(74) *Attorney, Agent, or Firm*—Gray, Cary, Ware & Freidenrich

(57) **ABSTRACT**

A self aligned method of forming a semiconductor memory array of floating gate memory cells in a semiconductor substrate has a plurality of spaced apart isolation regions on the substrate substantially parallel to one another. An active region is between each pair of adjacent isolation regions. The active and isolation regions are formed in parallel and in the column direction. In the row direction, strips of spaced apart silicon nitride are formed. A source line plug is formed between adjacent pairs of silicon nitride and is in contact with a first region in the active regions, and the isolation regions. The strips of silicon nitride are removed and isotropically etched. In addition, the materials beneath the silicon nitride are also isotropically etched. Polysilicon spacers are then formed in the row direction parallel to the source line plug and adjacent to the floating gates. A second region is formed between adjacent, spaced apart, control gates. A bit line is formed in the bit line direction contacting the second region in the space between the control gates.

19 Claims, 22 Drawing Sheets



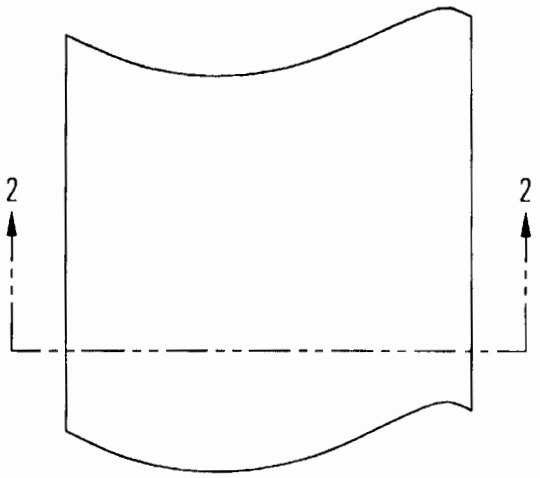


FIG. 1a–1

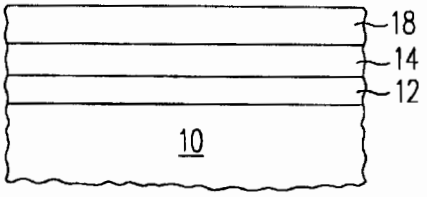


FIG. 1a–2

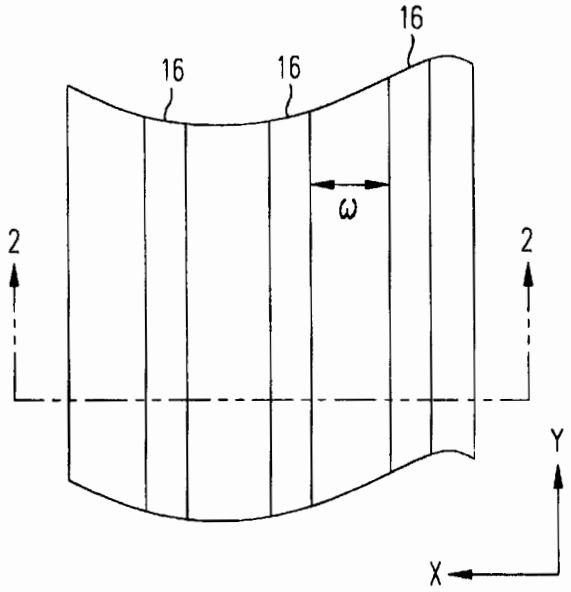


FIG. 1b–1

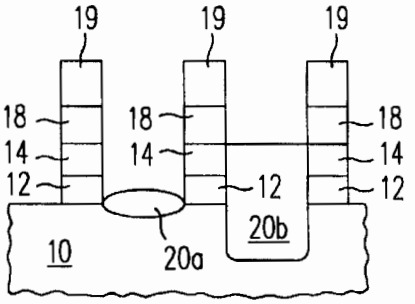


FIG. 1b–2

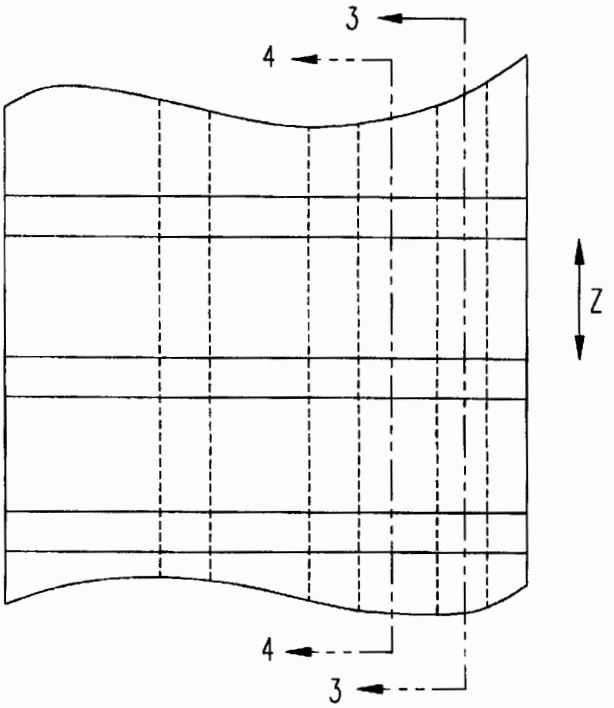


FIG. 1c-1

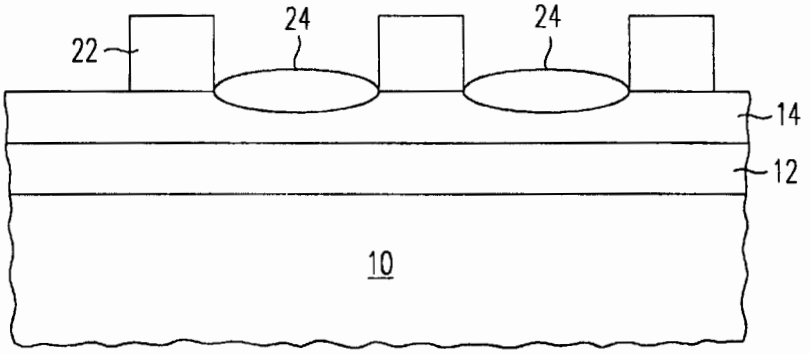


FIG. 1c-4

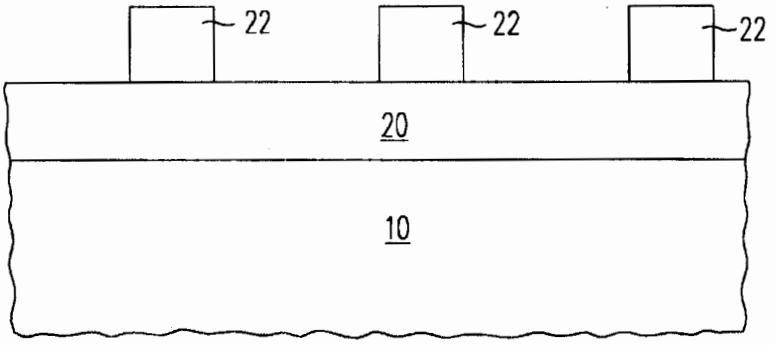


FIG. 1c-3

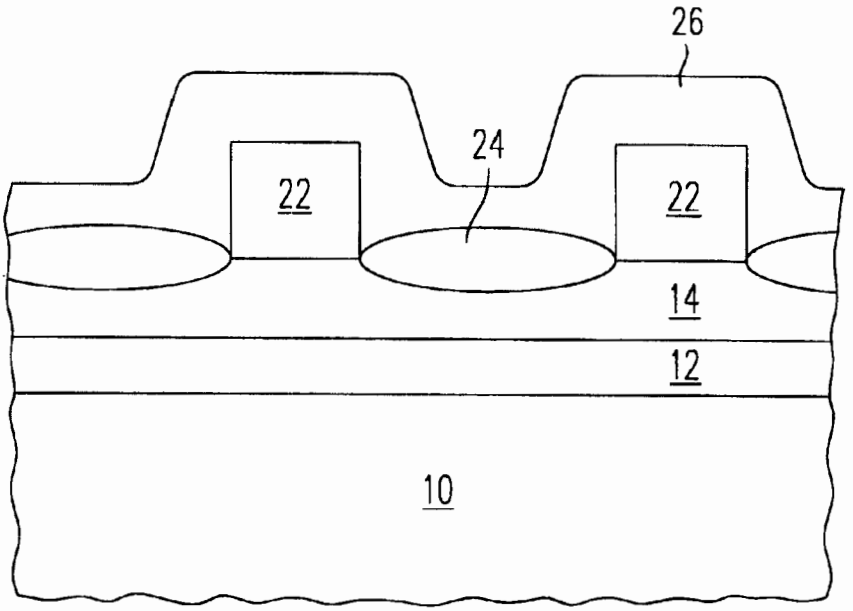


FIG. 2a–4

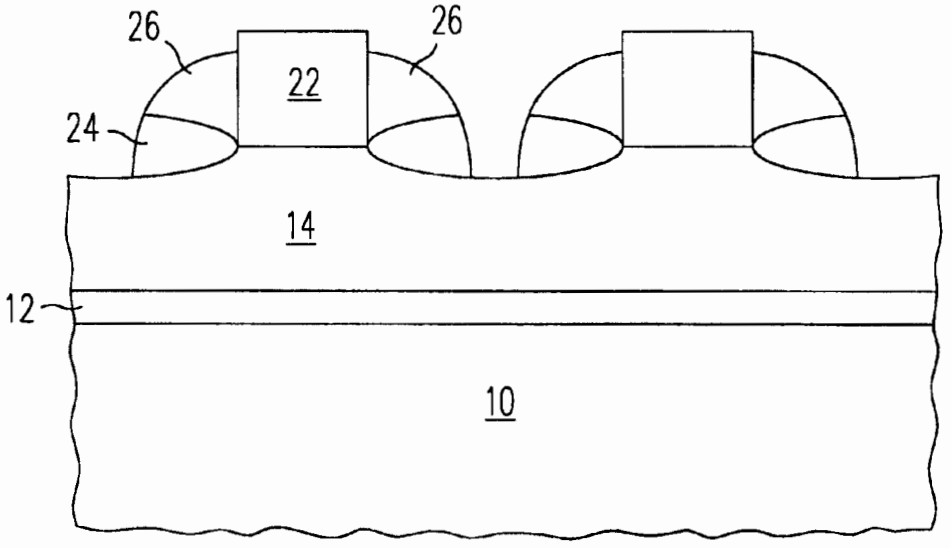


FIG. 2b–4

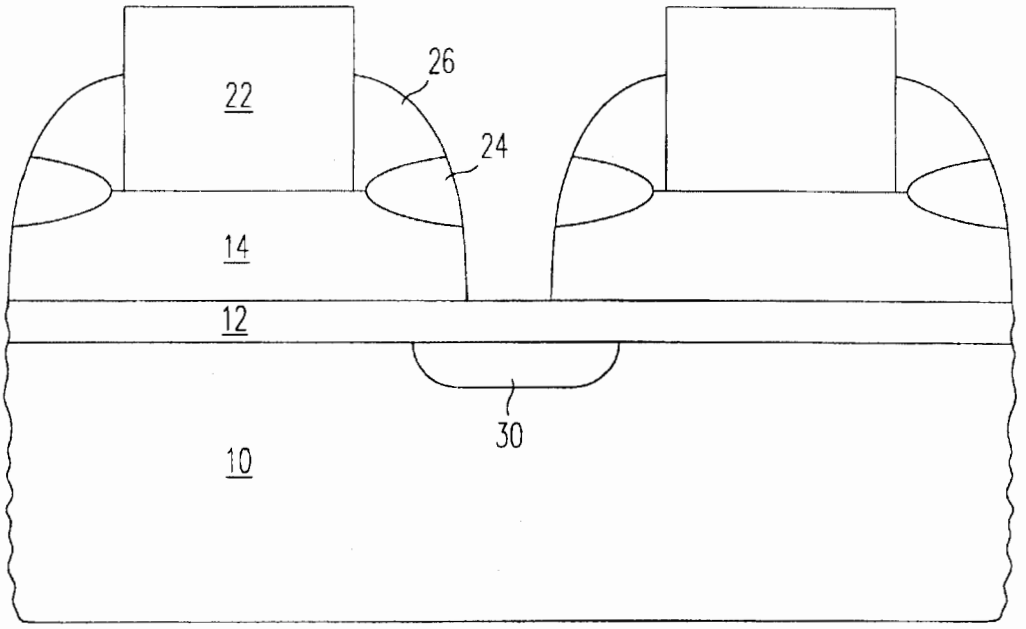


FIG. 2C–4

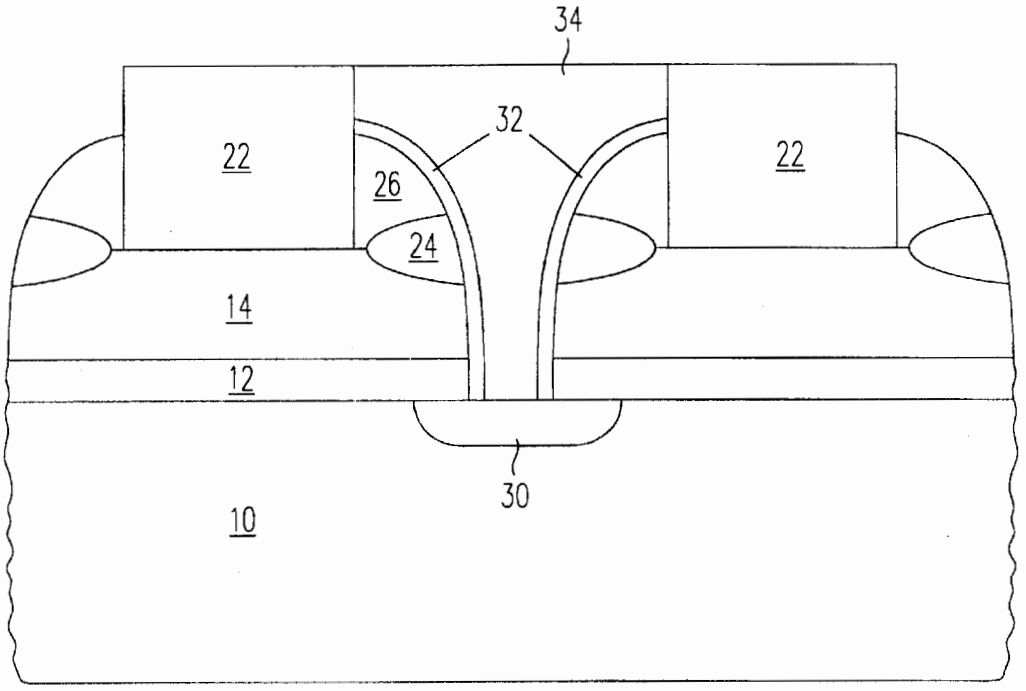


FIG. 2D–4

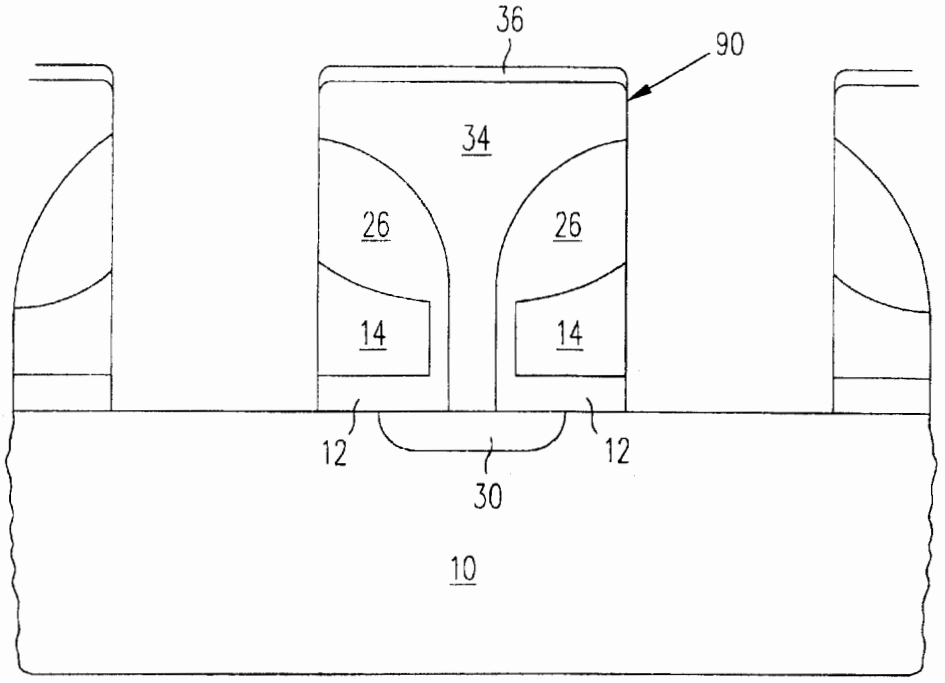


FIG. 2E-4

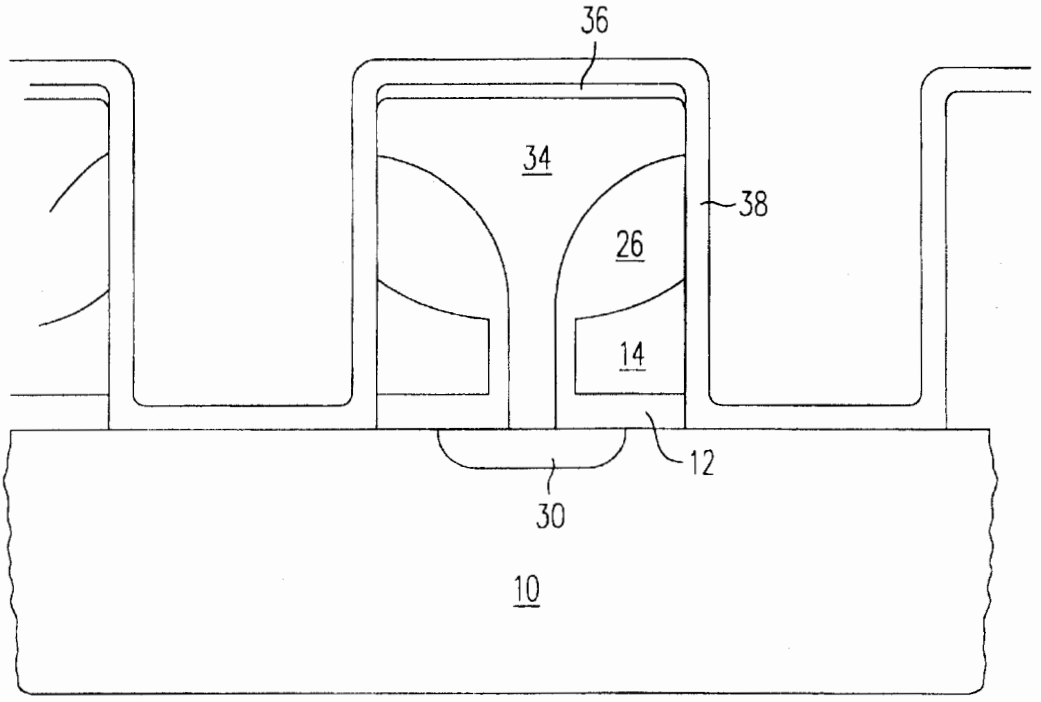


FIG. 2F-4

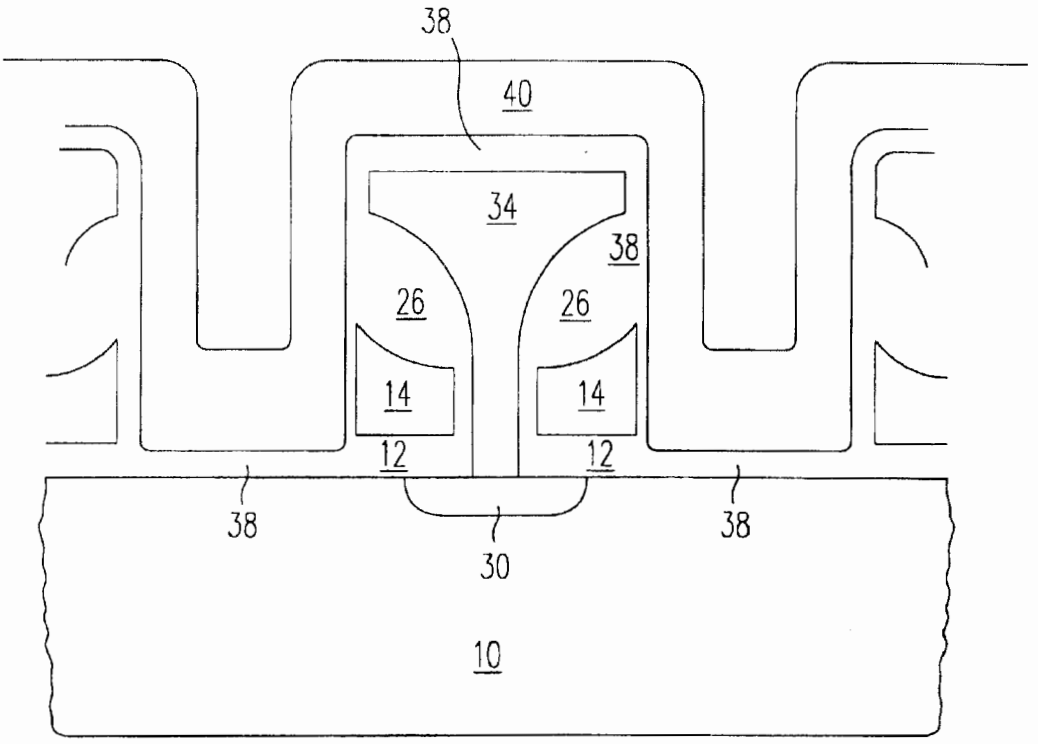


FIG. 2G-4

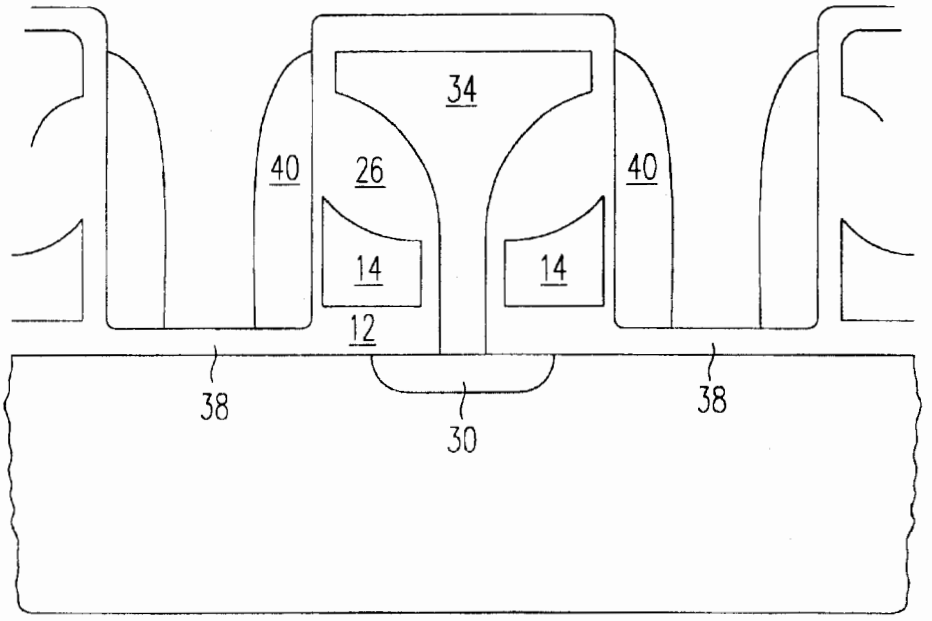


FIG. 2H-4

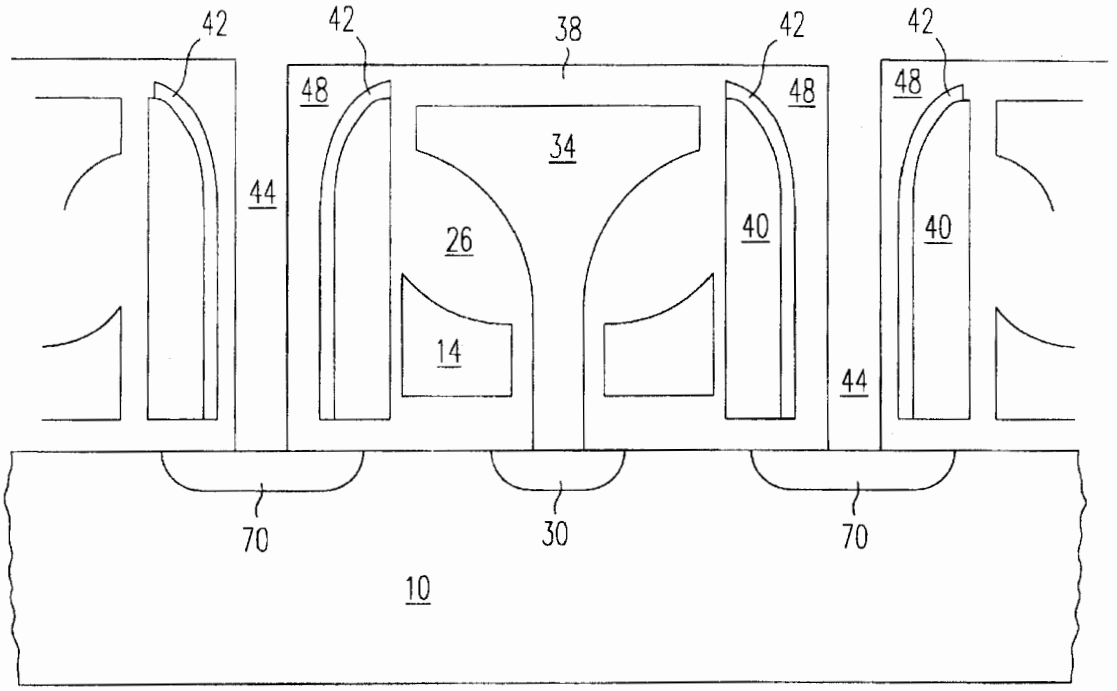


FIG. 2I–4

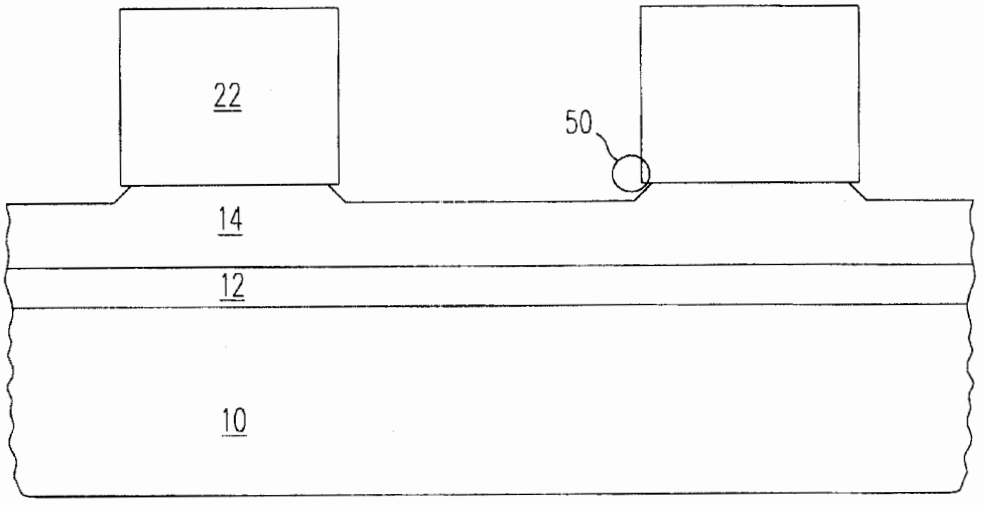


FIG. 3

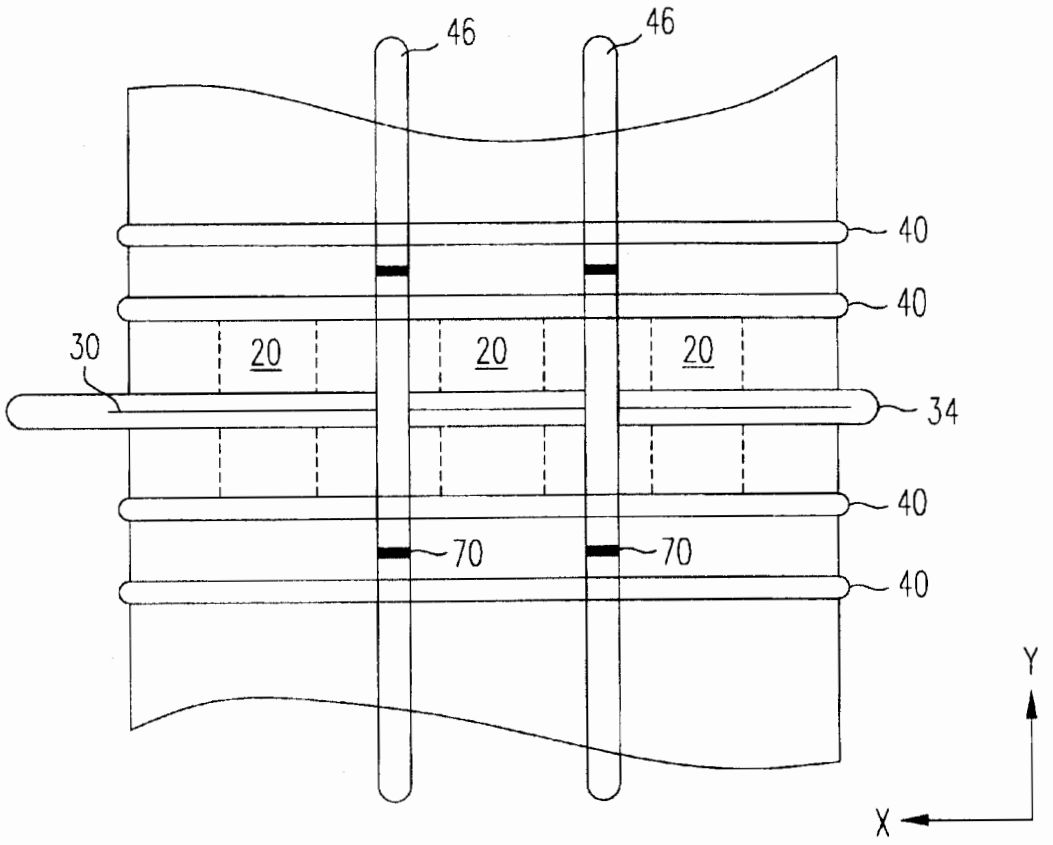


FIG. 2J-1

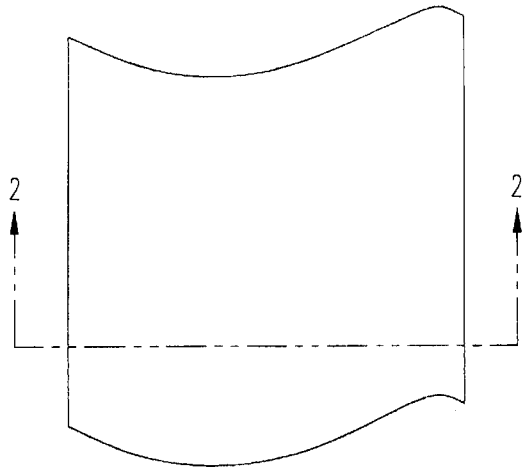


FIG. 4a-1

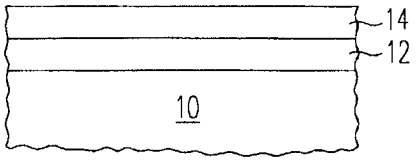


FIG. 4a-2

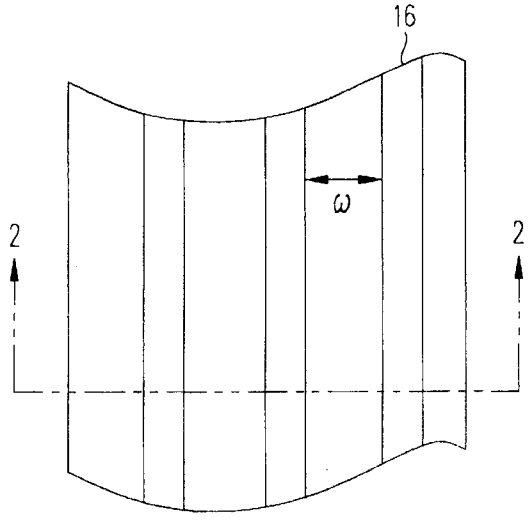


FIG. 4b-1

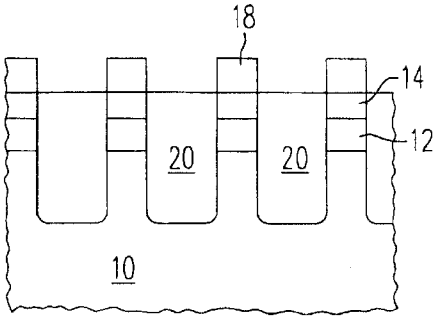


FIG. 4b-2

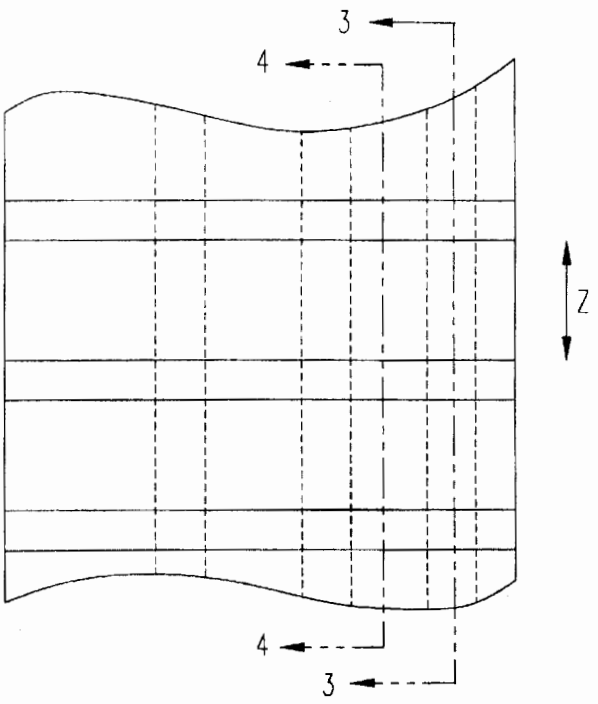


FIG. 4c–1

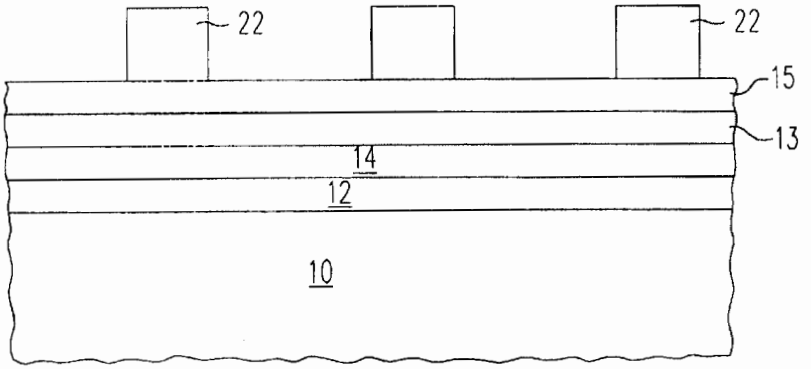


FIG. 4c–4

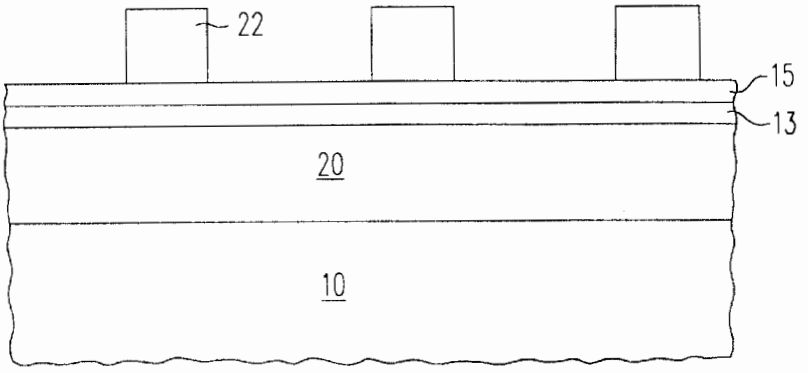


FIG. 4c–3

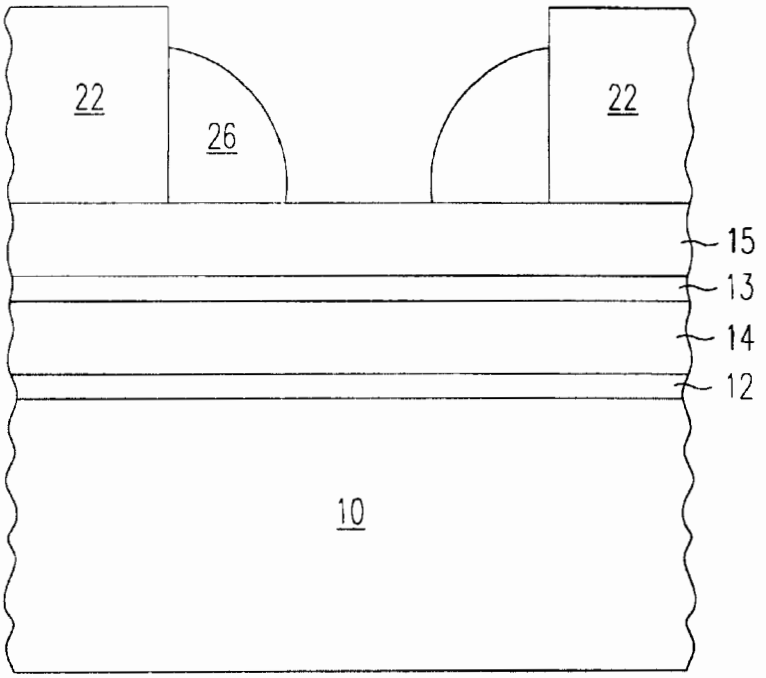


FIG. 5a–4

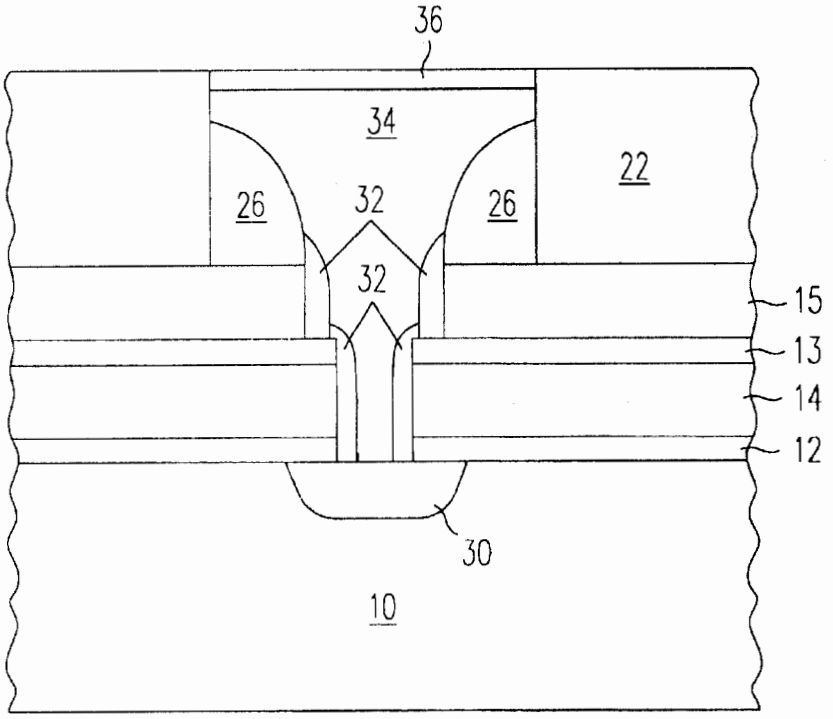


FIG. 5b–4

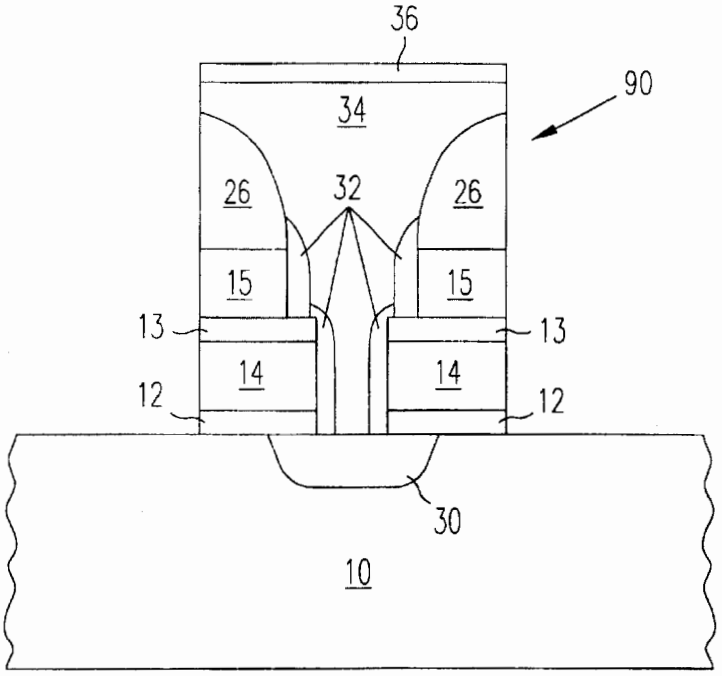


FIG. 5c-4

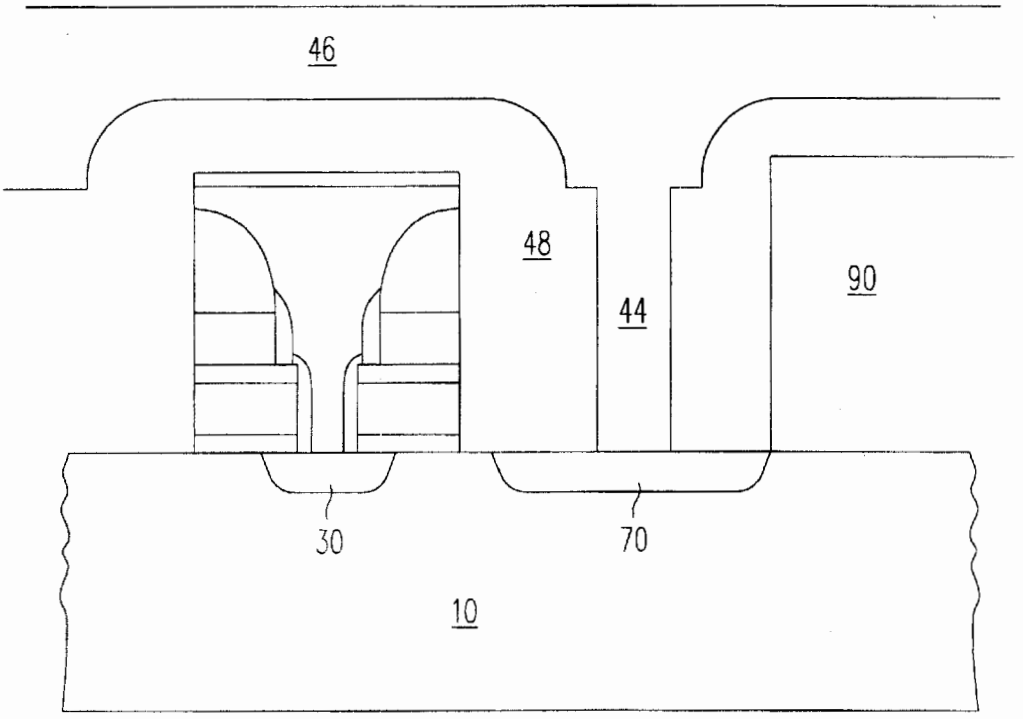


FIG. 5D-4

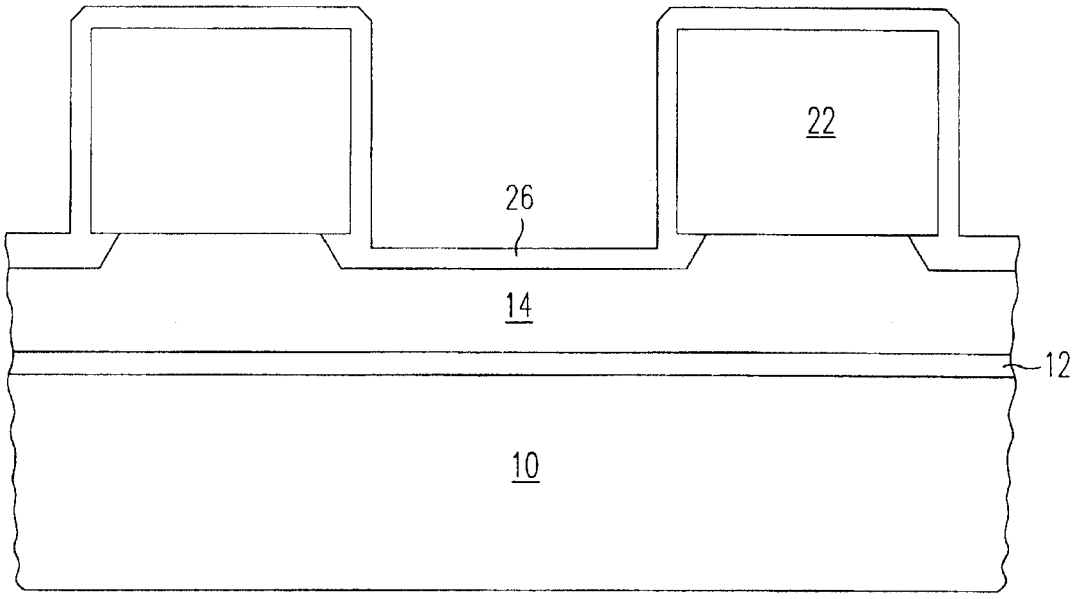


FIG. 6a-4

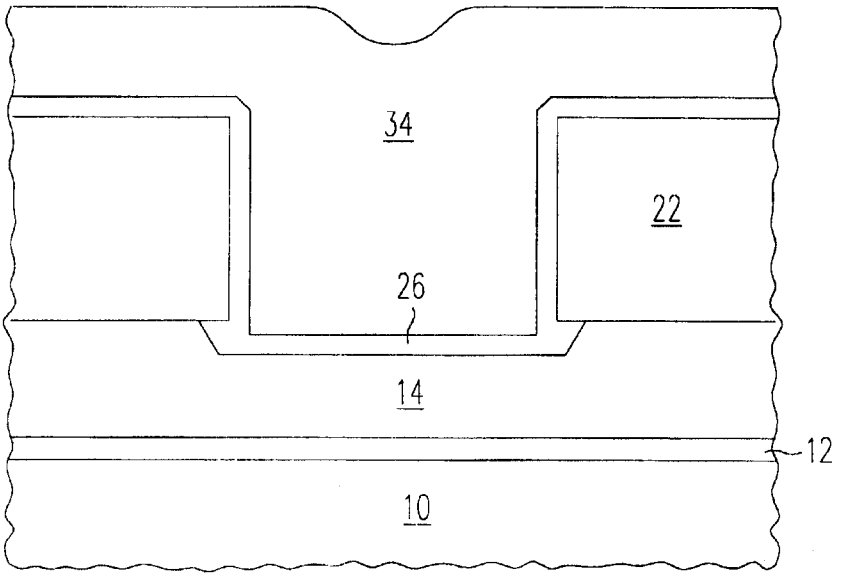


FIG. 6b-4

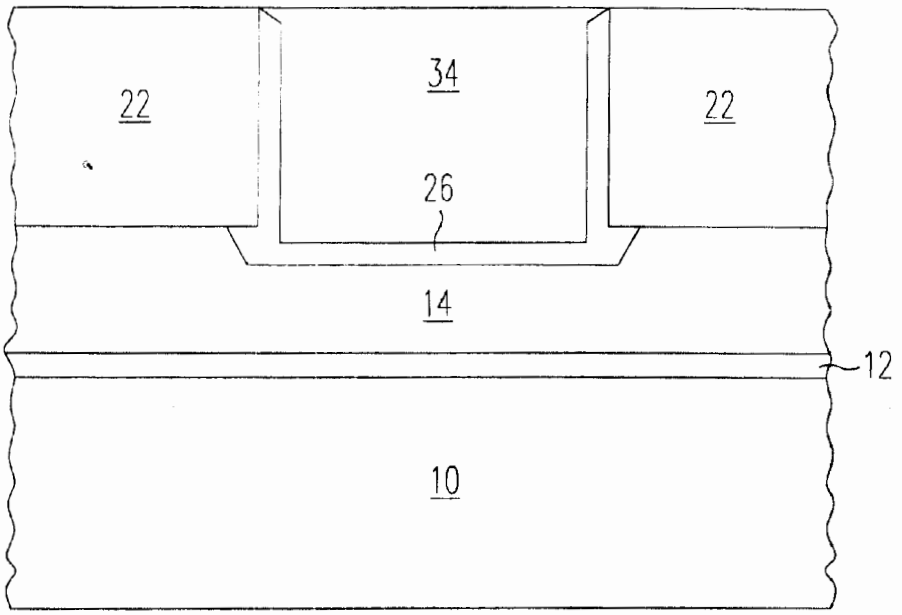


FIG. 6C-4

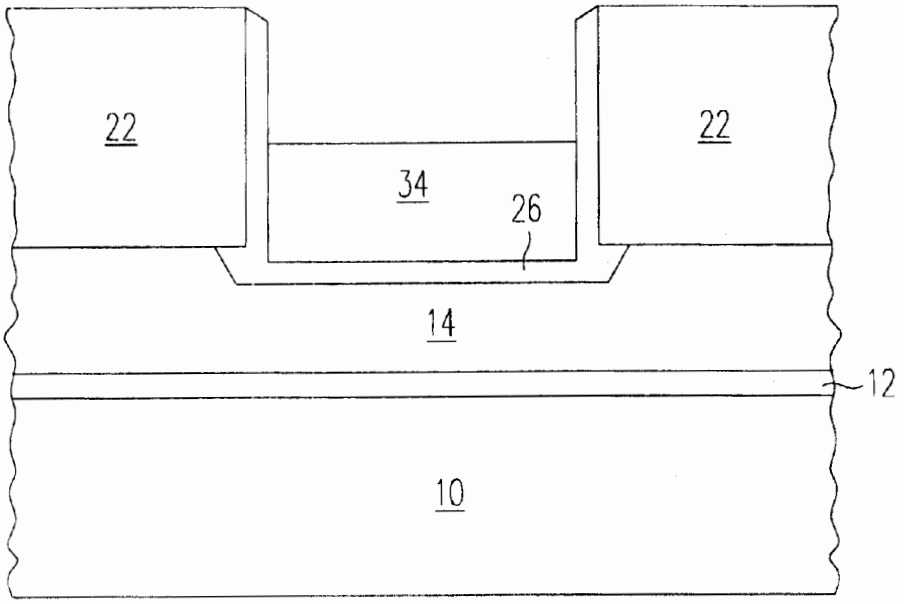


FIG. 6D-4

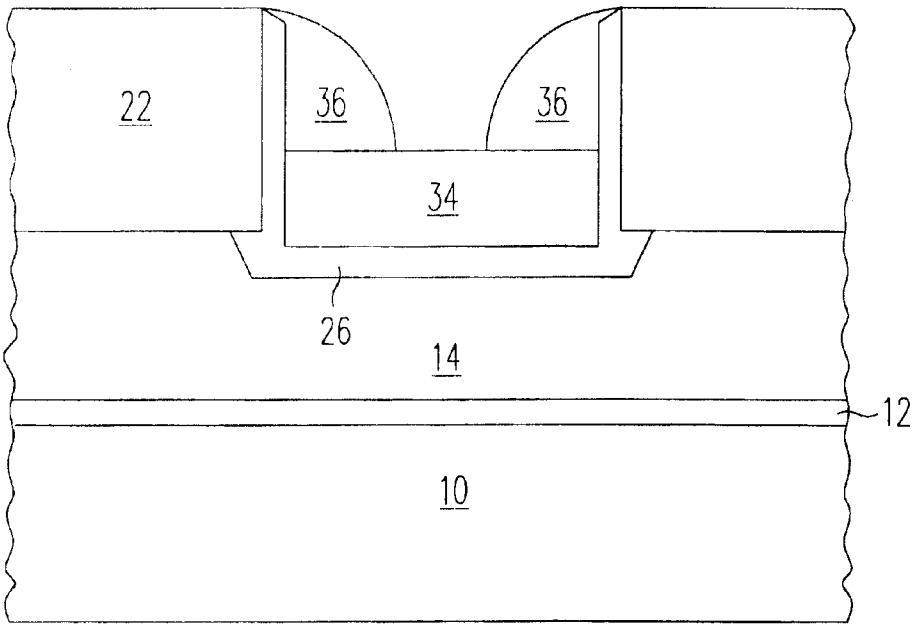


FIG. 6e-4

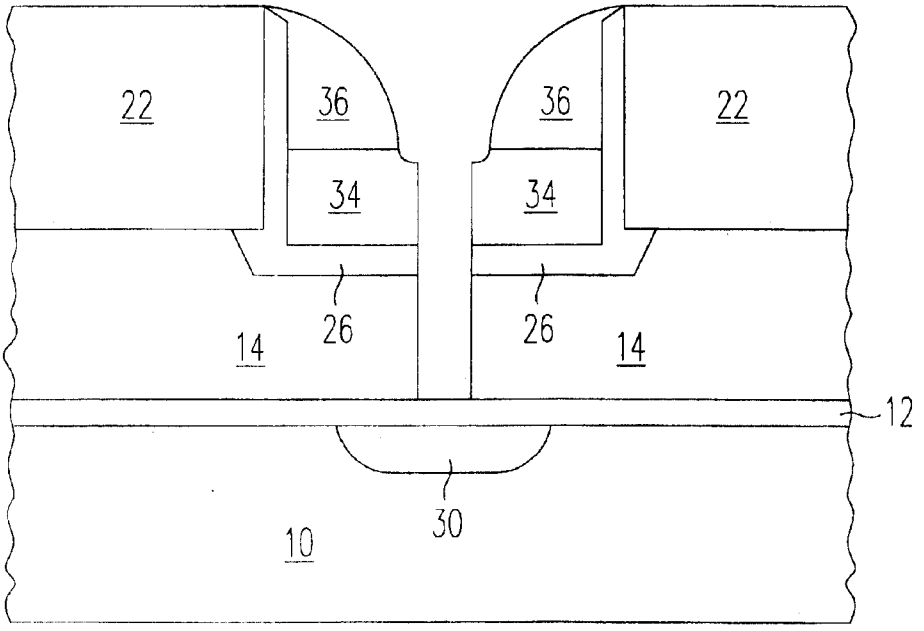


FIG. 6f-4

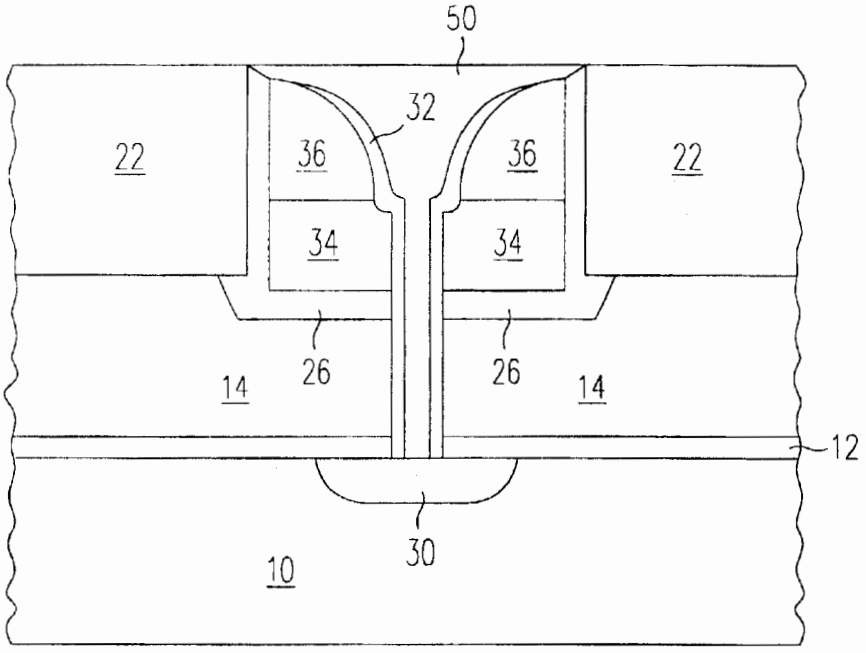


FIG. 6g-4

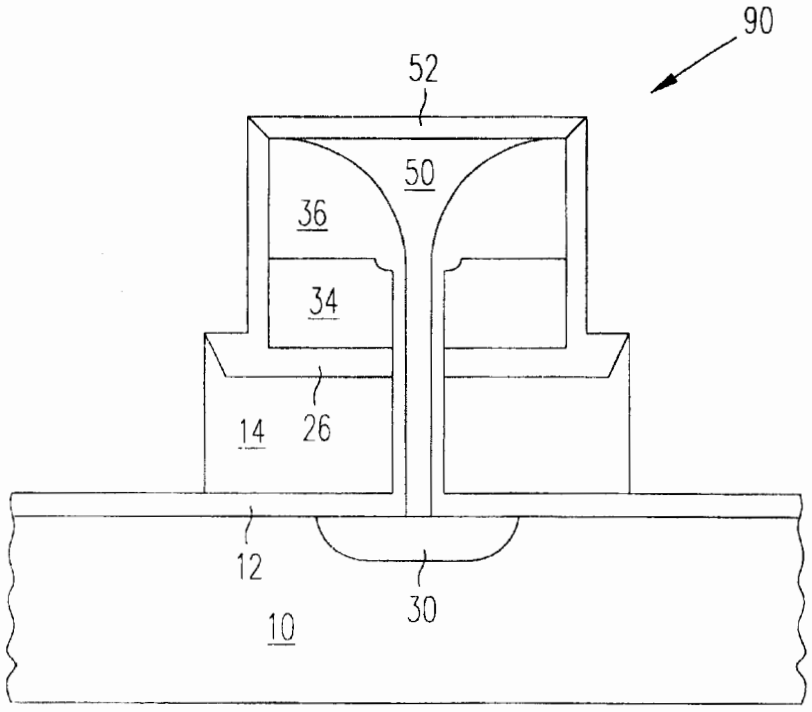


FIG. 6h-4

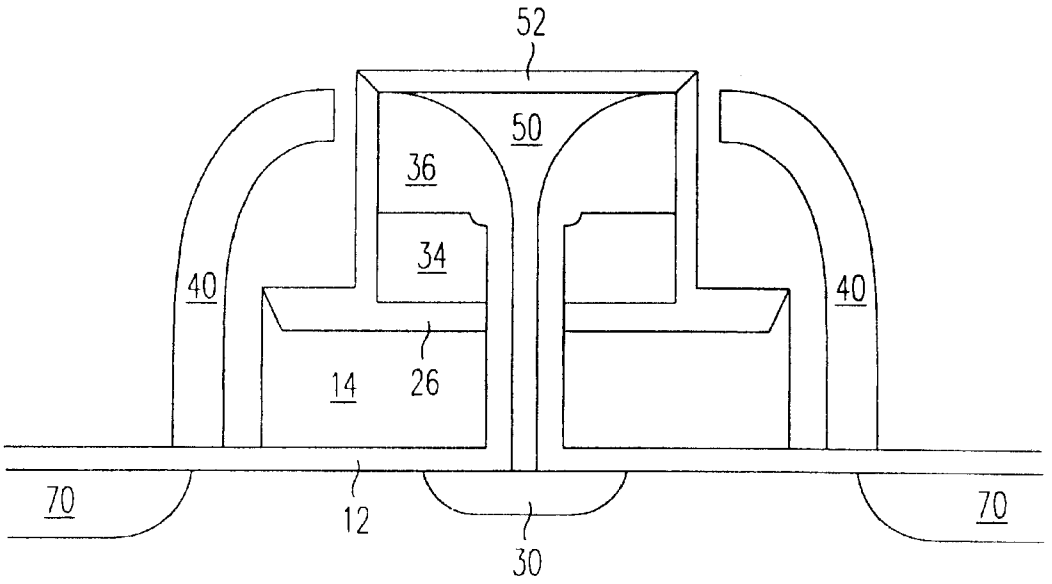


FIG. 6I-4

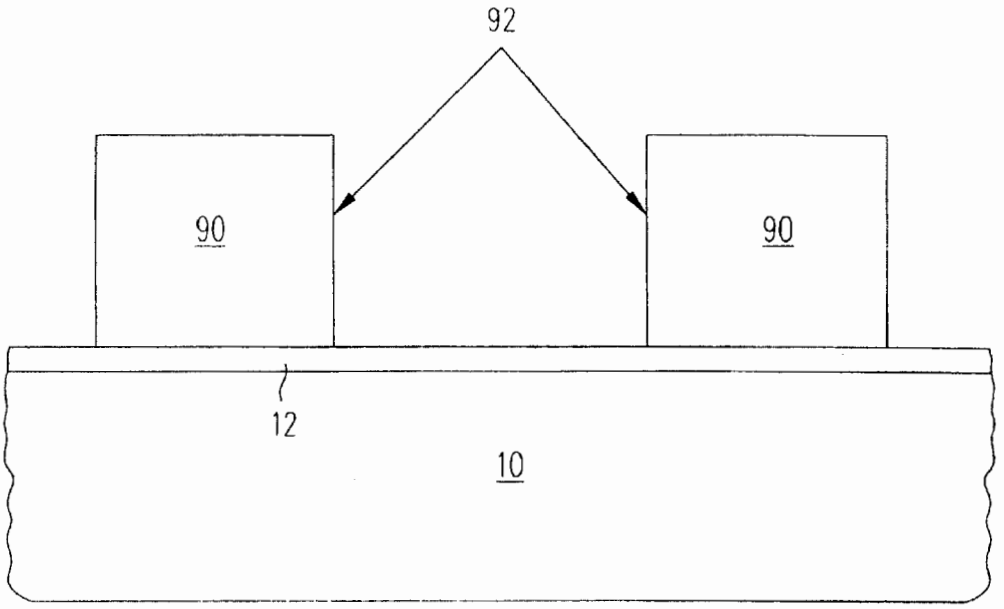


FIG. 7a-4

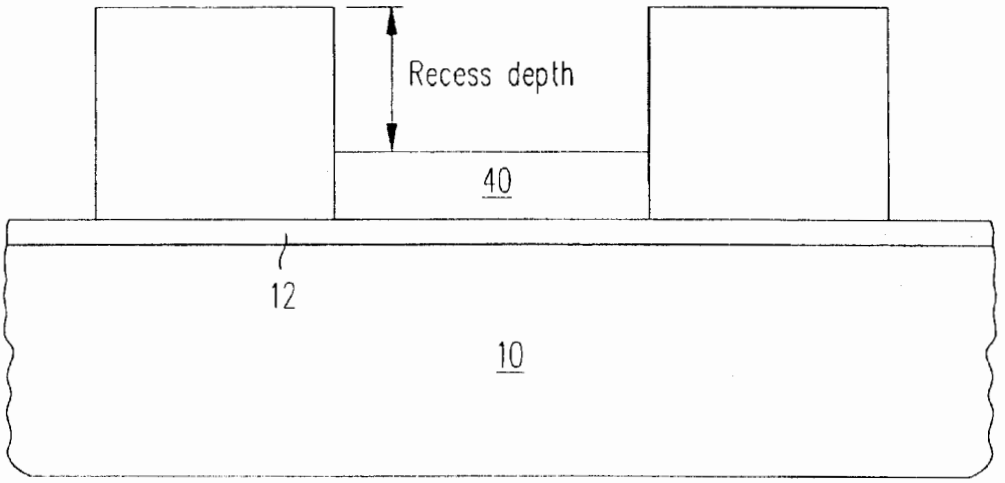


FIG. 7b-4

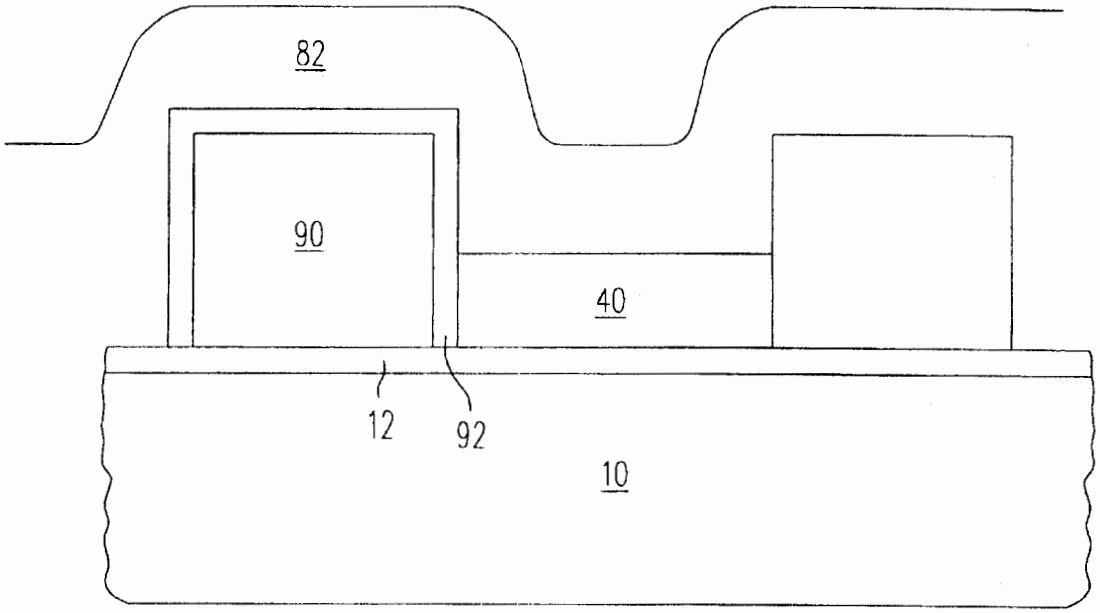


FIG. 7c–4

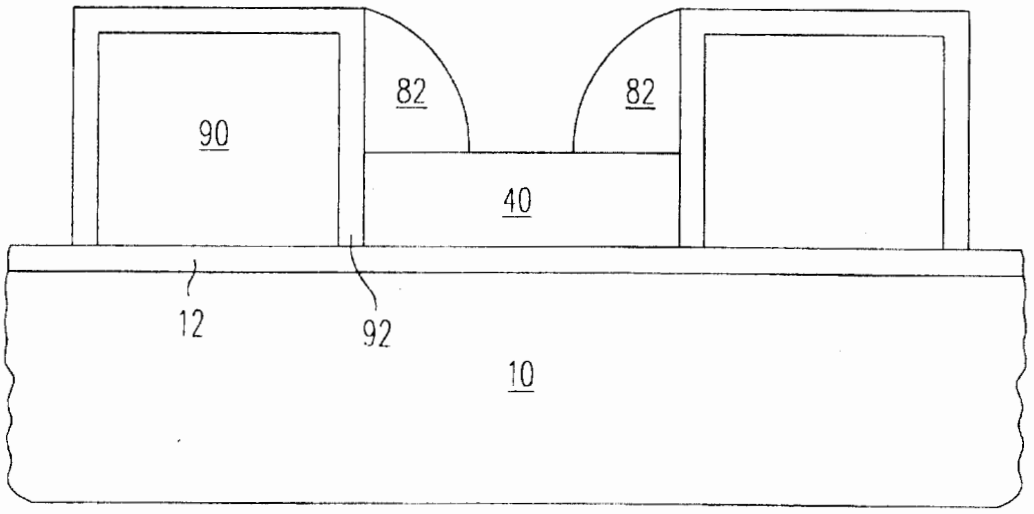


FIG. 7d–4

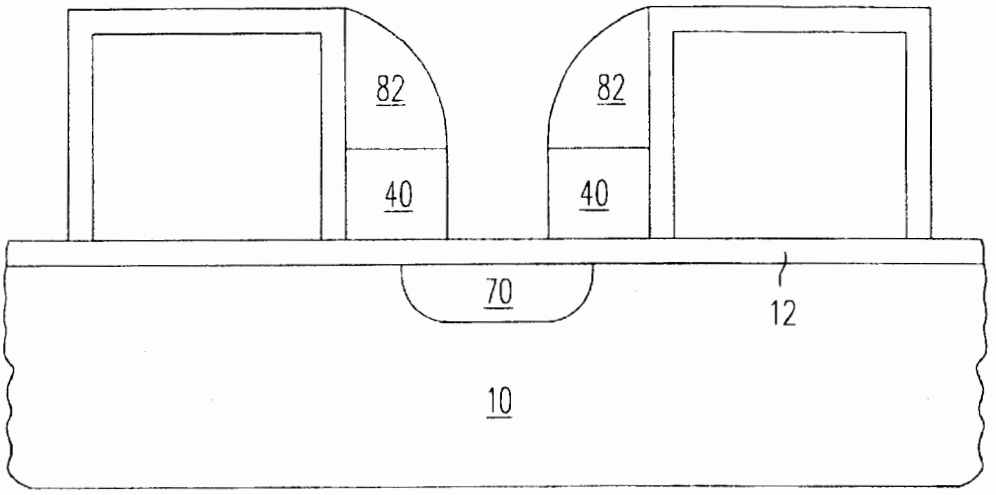


FIG. 7e-4

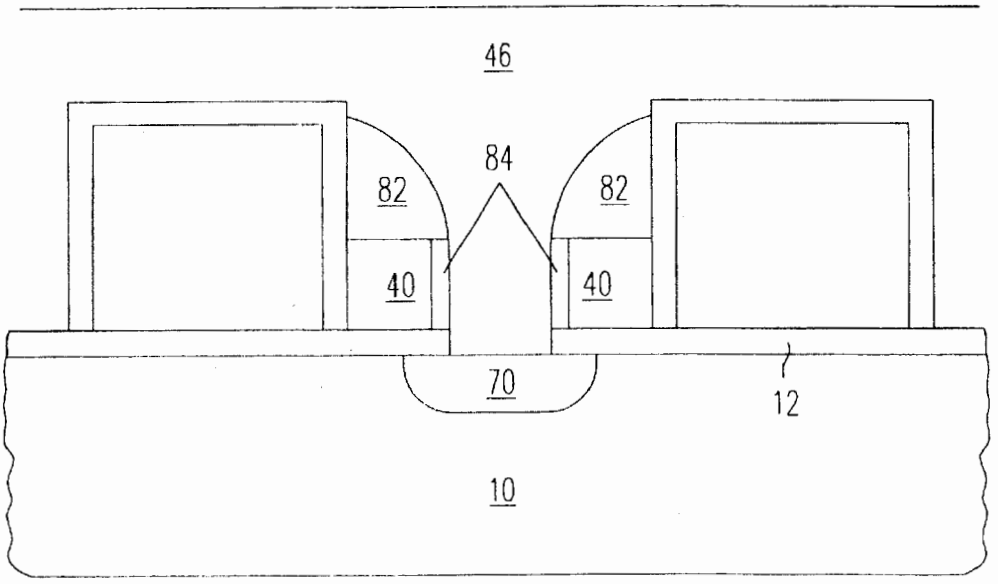


FIG. 7f-4

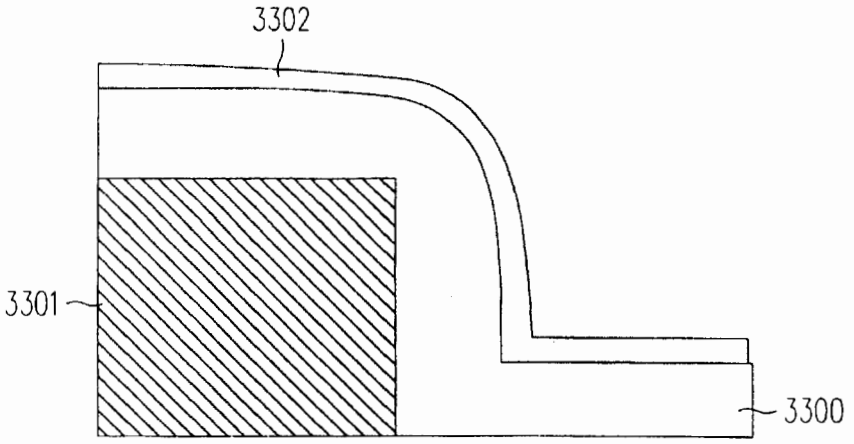


FIG. 8

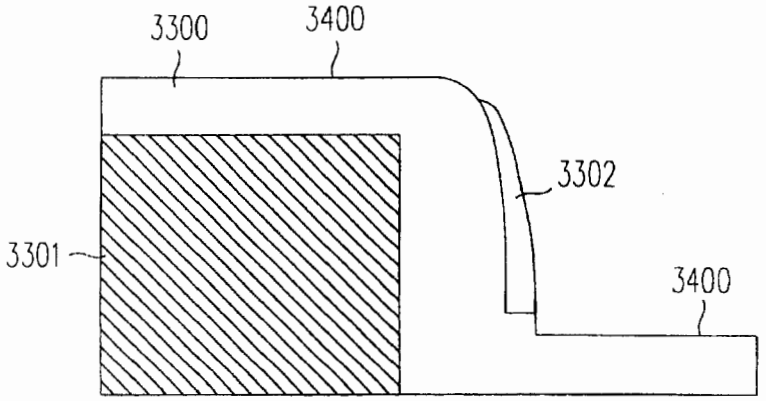


FIG. 9

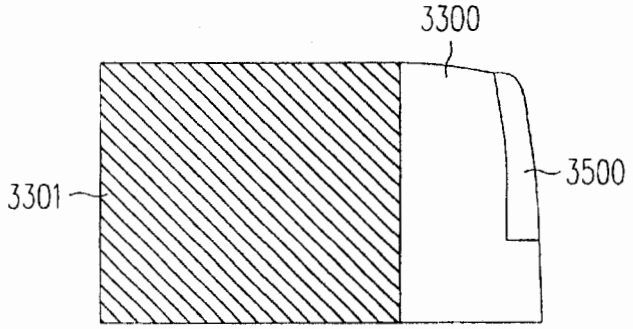


FIG. 10

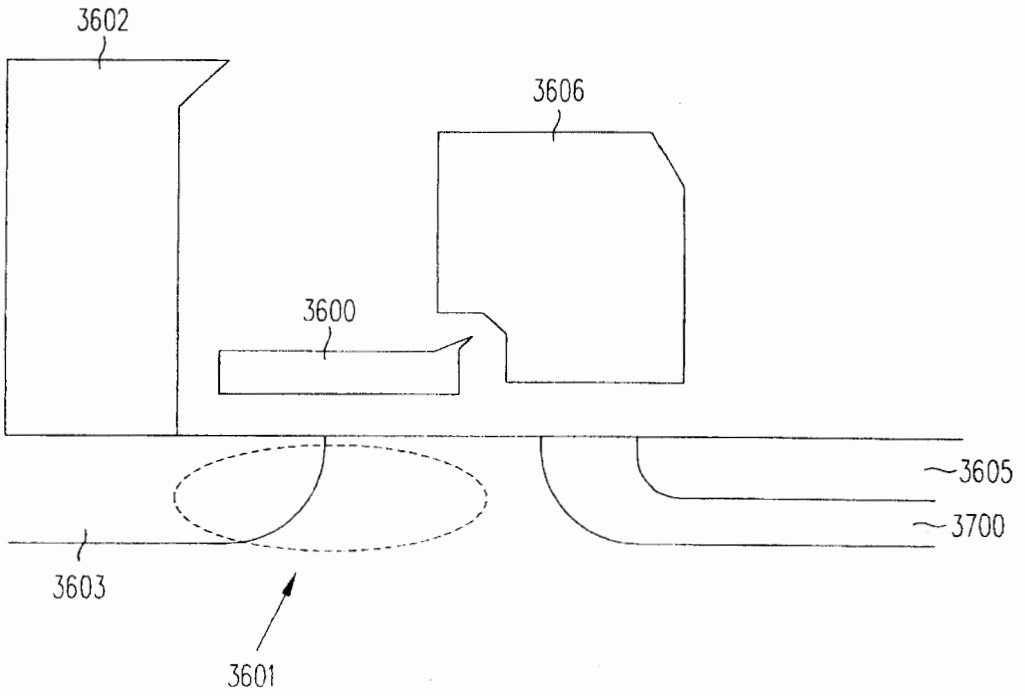


FIG. 11

SELF ALIGNED METHOD OF FORMING A SEMICONDUCTOR MEMORY ARRAY OF FLOATING GATE MEMORY CELLS, AND A MEMORY ARRAY MADE THEREBY

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a continuation of and claims the benefit of U.S. application Ser. No. 09/401,173, filed Sep. 22, 1999, the disclosure of which is incorporated herein by reference now U.S. Pat. No. 6,329,685.

TECHNICAL FIELD

The present invention relates to a self-aligned method of forming a semiconductor memory array of floating gate memory cells of the split gate type, stack gate type or a combination thereof. The present invention also relates to a semiconductor memory array of floating gate memory cells of the forgoing types.

BACKGROUND OF THE INVENTION

Non-volatile semiconductor memory cell using a floating gate to store charges thereon and memory arrays of such non-volatile memory cells formed in a semiconductor substrate are well known in the art. Typically, such floating gate memory cells have been of the split gate type, or stacked gate type, or a combination thereof.

One of the problems facing the manufacturability of semiconductor floating gate memory cell arrays has been the alignment of the various components such as source, drain, control gate, and floating gate. As the scale of integration of semiconductor processing increases, reducing the largest lithographic feature, the need for precise alignment becomes more critical. Alignment of various parts also determines the yield of the manufacturing of the semiconductor products.

Self-alignment is well known in the art. Self-alignment refers to the act of processing one or more steps involving one or more materials such that the features are automatically aligned with respect to one another in that step processing. Accordingly, the present invention uses the technique of self-alignment to achieve the manufacturing of a semiconductor memory array of the floating gate memory cell type.

SUMMARY OF THE INVENTION

In the present invention, three self-aligned methods are disclosed to form semiconductor memory arrays of floating gate memory cells of the split gate type, stacked gate type, and a combination thereof, as well as such memory arrays formed thereby. In the self aligned method of forming a semiconductor memory array of floating gate memory cells of the split gate type, the memory cell has a first terminal, a second terminal with a channel between the first terminal and the second terminal, a floating gate, and a control gate. In the method, a plurality of spaced apart isolation regions are formed in the substrate. The isolation regions are substantially parallel to one another in a first direction with an active region between each pair of adjacent isolation regions. Each active region has a first layer of insulating material on the semiconductor substrate, and a first layer of polysilicon material on the first layer of insulating material. A plurality of spaced apart masking regions of a masking material are formed substantially parallel to one another on said semiconductor substrate in a second direction crossing a plurality of alternating active regions and isolation regions.

The second direction is substantially perpendicular to the first direction. Etching along the second direction under the masking material is then performed. A plurality of spaced apart first spacers of an insulating material are formed substantially parallel to one another in the second direction. Each of the first spacers is adjacent to and contiguous with one of the masking regions with a first region between each pair of adjacent first spacers. Each first spacer crossing a plurality of alternating active regions and isolation regions. Between each pair of adjacent first spacers in the first region, the material is etched. A first terminal is formed in the substrate in the active region between pairs of adjacent first spacers in the first region. A conductor is formed in the second direction between each pair of spaced apart first spacers, electrically connected to the first terminal in the substrate. The masking material is removed resulting in a plurality of spaced apart structures substantially parallel to one another in the second direction. An insulating film is formed about each of these structures. A plurality of spaced apart second spacers of polysilicon material substantially parallel to one another is formed in the second direction. Each second spacer is adjacent to and contiguous with one of the structures. A second region is between each pair of adjacent second spacers with each second spacer crossing a plurality of alternating active regions and isolation regions. Each of the second spacer electrically connects the control gates for the memory cells in the second direction. Between each pair of adjacent second spacers in the second region, the material is etched. A second terminal is formed in the substrate in each of the active regions between pairs of adjacent second spacers in the second region. Finally, a conductor is formed in a first direction substantially parallel to an active region and electrically connected to the second terminals in the first direction.

A semiconductor memory array of a floating gate memory cell of the split gate type is formed by the foregoing method.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1***a*-**1** is a top view of a semiconductor substrate used in the first step of the method of present invention to form isolation regions.

FIG. **1***a*-**2** is a cross sectional view taken along the line **2**—**2**.

FIG. **1***b*-**1** is a top view of the next step in the processing of the structure of FIG. **1***a*-**1**, in which isolation regions are formed.

FIG. **1***b*-**2** is a cross sectional view taken along the line **2**—**2** showing the two types of isolation region that can be formed in the semiconductor substrate: LOCOS or shallow trench.

FIG. **1***c*-**1** is a top view showing the next step in the processing of the structure shown in FIG. **1***b*-**1** to form isolation regions.

FIG. **1***c*-**3** is a cross sectional view taken along the line **3**—**3**.

FIG. **1***c*-**4** is a cross sectional view taken along the line **4**—**4**.

FIG. **2***a*-**4** is a cross sectional view taken along the line **4**—**4** in the next step in the processing of the structure shown in FIG. **1***c*-**1**, in the formation of non volatile memory array of floating memory cells of the split gate type.

FIG. **2***b*-**4** is a cross sectional view taken along the line **4**—**4** in the next step in the processing of the structure shown in FIG. **2***a*-**4**, in the formation of non volatile memory array of floating memory cells of the split gate type.

FIG. **2***c*-**4** is a cross sectional view taken along the line **4**—**4** in the next step in the processing of the structure shown in FIG. **2***b*-**4**, in the formation of non volatile memory array of floating memory cells of the split gate type.

FIG. **2***d*-**4** is a cross sectional view taken along the line **4**—**4** in the next step in the processing of the structure shown in FIG. **2***c*-**4**, in the formation of non volatile memory array of floating memory cells of the split gate type.

FIG. **2***e*-**4** is a cross sectional view taken along the line **4**—**4** in the next step in the processing of the structure shown in FIG. **2***d*-**4**, in the formation of non volatile memory array of floating memory cells of the split gate type.

FIG. **2***f*-**4** is a cross sectional view taken along the line **4**—**4** in the next step in the processing of the structure shown in FIG. **2***e*-**4**, in the formation of non volatile memory array of floating memory cells of the split gate type.

FIG. **2***g*-**4** is a cross sectional view taken along the line **4**—**4** in the next step in the processing of the structure shown in FIG. **2***f*-**4**, in the formation of non volatile memory array of floating memory cells of the split gate type.

FIG. **2***h*-**4** is a cross sectional view taken along the line **4**—**4** in the next step in the processing of the structure shown in FIG. **2***g*-**4**, in the formation of non volatile memory array of floating memory cells of the split gate type.

FIG. **2***i*-**4** is a cross sectional view taken along the line **4**—**4** in the next step in the processing of the structure shown in FIG. **2***h*-**4**, in the formation of non volatile memory array of floating memory cells of the split gate type.

FIG. **2***j*-**1** is a top view showing the interconnection of row lines and bit lines to terminals in active regions in the formation of the non volatile memory array of floating memory cells of the split gate type.

FIG. **3** is a cross sectional view taken along the line **4**—**4**, and is similar to FIG. **1***c*-**4** showing the result of a variation in the processing step to form an undercut in the insulating material.

FIG. **4***a*-**1** is a top view of a semiconductor substrate used in the first step of the method of present invention to form isolation regions in an array of non-volatile memory cells with floating gate memory cells of the stacked gate type.

FIG. **4***a*-**2** is a cross sectional view taken along the line **2**—**2** shown in FIG. **4***a*-**1**.

FIG. **4***b*-**1** is the next step in the formation of an array of floating gate memory cells of the stacked gate type in which isolation regions are formed in the structure of FIG. **4***a*-**1**.

FIG. **4***b*-**2** is a cross sectional view taken along the line **2**—**2** shown in FIG. **4***a*-**1** showing the isolation regions and active regions.

FIG. **4***c*-**1** is a top view showing the next step in the formation of a non volatile memory array of the stacked gate type.

FIG. **4***c*-**3** is a cross sectional view taken along the line **3**—**3** of the structure shown in FIG. **4***c*-**1**.

FIG. **4***c*-**4** is a cross sectional view taken along the line **4**—**4** of the structure shown in FIG. **4***c*-**1**.

FIG. **5***a*-**4** is a cross sectional view taken along the line **4**—**4** in the next step in the formation of the non volatile memory array of floating memory cells of the stacked gate type.

FIG. **5***b*-**4** is a cross sectional view taken along the line **4**—**4** showing the next step in processing the structure shown in FIG. **5***a*-**4**, in the formation of the non volatile memory array of floating memory cells of the stacked gate type.

FIG. **5***c*-**4** is a cross sectional view taken along the line **4**—**4** showing the next step in processing the structure shown in FIG. **5***b*-**4** in the formation of the non volatile memory array of floating memory cells of the stacked gate type.

FIG. **5***d*-**4** is a cross sectional view taken along the line **4**—**4** showing the next step in processing the structure shown in FIG. **5***c*-**4** in the formation of the non volatile memory array of floating memory cells of the stacked gate type in which bit line and drain regions are formed.

FIG. **6***a*-**4** is a cross sectional view taken along the line **4**—**4** showing the result of processing the structure shown in FIG. **3**, in the formation of a non volatile memory array of floating gate memory cells of a combination of stacked gate and split gate type.

FIG. **6***b*-**4** is a cross sectional view taken along the line **4**—**4** showing the next step in processing the structure shown in FIG. **6***a***4**, in the formation of a non volatile memory array of floating gate memory cells of a combination of stacked gate and split gate type.

FIG. **6***c*-**4** is a cross sectional view taken along the line **4**—**4** showing the next step in processing the structure shown in FIG. **6***b*-**4**, in the formation of a non volatile memory array of floating gate memory cells of a combination of stacked gate and split gate type.

FIG. **6***d*-**4** is a cross sectional view taken along the line **4**—**4** showing the next step in processing the structure shown in FIG. **6***c*-**4**, in the formation of a non volatile memory array of floating gate memory cells of a combination of stacked gate and split gate type.

FIG. **6***e*-**4** is a cross sectional view taken along the line **4**—**4** showing the next step in processing the structure shown in FIG. **6***d*-**4**, in the formation of a non volatile memory array of floating gate memory cells of a combination of stacked gate and split gate type.

FIG. **6***f*-**4** is a cross sectional view taken along the line **4**—**4** showing the next step in processing the structure shown in FIG. **6***e*-**4**, in the formation of a non volatile memory array of floating gate memory cells of a combination of stacked gate and split gate type.

FIG. **6***g*-**4** is a cross sectional view taken along the line **4**—**4** showing the next step in processing the structure shown in FIG. **6***f*-**4**, in the formation of a non volatile memory array of floating gate memory cells of a combination of stacked gate and split gate type.

FIG. **6***h*-**4** is a cross sectional view taken along the line **4**—**4** showing the next step in processing the structure shown in FIG. **6***g*-**4** in the formation of a non volatile memory array of floating gate memory cells of a combination of stacked gate and split gate type.

FIG. **6***i*-**4** is a cross sectional view taken along the line **4**—**4** showing the next step in processing the structure shown in FIG. **6***h*-**4** in the formation of a non volatile memory array of floating gate memory cells of a combination of stacked gate and split gate type.

FIG. **7***a*-**4** is a cross sectional view taken along the line **4**—**4** showing the structure formed in FIG. **2***e*-**4**, **5***c*-**4**, or **6***h*-**4**, in the first step in the method of the present invention to form self-aligned bit lines.

FIG. **7***b*-**4** is a cross sectional view taken along the line **4**—**4** showing the next step in processing the structure shown in FIG. **7***a*-**4**, in the formation of self-aligned bit lines.

FIG. **7***c*-**4** is a cross sectional view taken along the line **4**—**4** showing the next step in processing the structure shown in FIG. **7***b*-**4**, in the formation of self-aligned bit lines.

FIG. **7***d*-**4** is a cross sectional view taken along the line **4**—**4** showing the next step in processing the structure shown in FIG. **7***c*-**4**, in the formation of self-aligned bit lines.

FIG. **7***e*-**4** is a cross sectional view taken along the line **4**—**4** showing the next step in processing the structure shown in FIG. **7***d*-**4**, in the formation of self-aligned bit lines.

FIG. **7***f*-**4** is a cross sectional view taken along the line **4**—**4** showing the next step in processing the structure shown in FIG. **7***e*-**4**, in the formation of self-aligned bit lines.

FIG. **8** is a cross sectional view of a drawing of the polysilicon/oxide stacking for the formation of a square spacer;

FIG. **9** is a cross sectional view of the etch breaking through the oxide on planar surfaces and forming an oxide spacer on the sidewall;

FIG. **10** is a cross sectional view of the oxide spacer slowing the polysilicon etch at the corner producing a square spacer;

FIG. **11** is a schematic drawing of a single well split gate non-volatile memory cell made by the method of the present invention having a halo.

DETAILED DESCRIPTION OF THE DRAWINGS

Referring to FIG. **1***a*-**1** there is shown a top plan view of a semiconductor substrate **10** having a first layer of insulating material **12**, such as silicon dioxide deposited thereon. A first layer of polysilicon **14** is deposited on the first layer of insulating material **12**. The semiconductor substrate **10** is preferably of P type and is well known in the art. The first insulating layer **12** is formed on the substrate **10** by well known techniques such as oxidation or deposition (e.g. chemical vapor deposition or CVD), forming a layer of silicon dioxide of approximately 80–90 Å in thickness. Similarly, the deposition and formation of the first polysilicon layer **14** on the first insulating layer **12** can be made by well known process such as Low Pressure CVD or LPCVD resulting in a layer of approximately 500–700 Å thickness of polysilicon **14** on the first insulating layer **12**. A silicon nitride layer **18** of preferably 500 Å is deposited by CVD. This layer **18** is used to define the active regions during isolation formation. Of course, all of the forgoing described parameters and the parameters described hereinafter, depend upon the design rules and the process technology generation. What is described herein is for the 0.18 micron process. However, it will be understood by those skilled in the art that the present invention is not limited to any specific process technology generation, nor to any specific value in any of the process parameters described hereinafter.

Once the first insulating layer **12**, the first polysilicon layer **14**, and the silicon nitride **18** have been formed, suitable photo-resistant material **19** is applied on the silicon nitride layer **18** and a masking step is performed to etch the silicon nitride **18**, the first polysilicon **14**, and the underlying first insulating layer **12** in selective regions. Where the photo resist **19** is not removed, they remain on top of the silicon nitride **18**, the first polysilicon region **14** and the underlying insulating region **12**. Where the photo-resist material **19** is removed, the silicon nitride **18**, the polysilicon **14** and the underlying insulating material **12** are etched away in strips **16** formed in the Y direction or the column direction, as shown in FIG. **1***b*-**1**. (As will be described, there are two embodiments in the formation of the isolation regions: LOCOS and STI. In the STI embodiment, the etching continues into the substrate **10** to a depth of approximately 2800 Å). The distance W between adjacent strips **16** can be as small as the smallest lithographic feature of the process used.

After the silicon nitride **18**, the first polysilicon **14** and the first insulating layer **12** are etched away in strips **16**, the regions or "grooves" **16** in the semiconductor substrate **10** are filled with an isolation material **20***a* or **20***b*, such as silicon dioxide. As shown in FIG. **1***b*-**2**, this can be the well known LOCOS process resulting in the local field oxide **20***a* or it can be a shallow trench process (STI) resulting in silicon-dioxide being formed in the region **20***b*. Where the photo-resist **19** has not been removed, the semiconductor substrate **10** beneath the silicon nitride **18**, the first polysilicon **14** and the underlying first insulating material **12** forms the active region. Thus, at this point, the substrate **10** has alternating strips of active regions and isolation regions with the isolation region being formed of either LOCOS **20***a* or shallow trench **20***b*. It should be noted that although FIG. **1***b*-**2** shows the formation of both a LOCOS region **20***a* and a shallow trench region **20***b*, only one of either the LOCOS process **20***a* or the shallow trench **20***b* will be used. In the preferred embodiment, the shallow trench **20***b* will be formed. Shallow trench **20***b* is desirable because it can be formed planar with respect to the first polysilicon layer **14**. The structure at this point represents a self-aligned floating gate to active.

This structure is more compact than a structure formed by a non self-aligned method. A non self-aligned method of forming the structure shown in FIG. **1***b*, which is well known and is conventional, is as follows. Regions of isolation **20** are first formed in the substrate **10**. This can be done by depositing a layer of silicon nitride on the substrate **10**, depositing photoresist patterning the silicon nitride to expose selective portions of the substrate **10**, and then oxidizing the exposed substrate **10** using either the LOCOS process or the STI process. Thereafter, the silicon nitride is removed, and a first layer of silicon dioxide **12** (to form the gate oxide) is deposited over the substrate **10**. A first layer of polysilicon **14** is deposited over the gate oxide **12**. The first layer of polysilicon **14** is then patterned and selective portions removed. Thus, the polysilicon **14** is not self aligned with the regions of isolation **20**, and a second masking step is required. Further, the additional masking step requires that the dimensions of the polysilicon **14** have an alignment tolerance with respect to the regions of isolation **20**.

With the structure shown in FIG. **1***b* made using either the self aligned method or the non self-aligned method, the structure is further processed as follows.

Referring to FIG. **1***c*-**1**, there is shown the top view of the next step in the process of the present invention. A masking layer **22**, such as silicon nitride **22**, is applied across the entire surface of the structure shown in FIG. **1***b*-**1**. A second masking operation is performed with photo-resist applied on top of the silicon nitride **22**. A mask in which strips are defined in the X or the row direction is applied. The distance Z between adjacent strips can be a size determined by the needs of the device to be fabricated. The proposed structure can contain three "features", i.e. two gates and one "space" within the distance Z. The photo resist is removed in selective regions, i.e. strips in the row direction. The exposed masking material, or silicon nitride **22** is then etched, resulting in the structure shown in FIG. **1***c*-**1**. In the process, each strip of silicon nitride **22** crosses over an active region in the semiconductor substrate **10** over which lies a first insulating layer **12** and a polysilicon layer **14**, and over an isolation region in the semiconductor substrate **10**, consisting of the shallow trench silicon dioxide **20**. In addition, between each strips of silicon nitride **22** is a groove crossing over the shallow trench **20** and over an oxidized region of

the first polysilicon **14**, shown as **24** in FIG. **1***c*-**4**. The material **24** is the same silicon dioxide as that which is formed as the isolation region **20** in the shallow trench. The formation of the strips of silicon nitride **22** can be as follows:

The silicon nitride **22** is applied on the structure shown in FIG. **1***b*-**1** by CVD in which a layer of approximately 3000 Å in thickness of silicon nitride **22** is formed on the structure.

Thereafter the silicon nitride **22** is etched selectively. The first polysilicon layer **14** and silicon dioxide regions **20***a* or **20***b* form etch stops thereby stopping the etching process. Finally, the exposed first polysilicon **14** is then oxidized to form the silicon dioxide **24**.

A second layer **26** of insulating material, such as silicon dioxide deposited from the decomposition of tetraethylorthosilicate (TEOS) is then applied on the entire surface of the structure shown in FIG. **1***c*-**1**. A cross sectional view of the layer **26** of TEOS applied on the entire structure is shown in FIG. **2***a*-**4**. The TEOS **26** can be applied using conventional processes such as CVD or conformal deposition to a thickness of approximately 2000–2500 Å.

The layer of TEOS **26** is then anisotropically etched, by well known techniques, such as Reactive Ion Etch (RIE), until it no longer "covers" the strips of silicon nitride **22**. As a result, strips of spacers **26** of TEOS **26** border and are adjacent to each strip of silicon nitride **22**. This is shown in FIG. **2***b*-**4**. The anisotropic etching of the TEOS **26** continues until the etch stop silicon nitride **22** and the first polysilicon **14** are observed.

Thereafter, the etchant is changed to etch the first polysilicon **14**. Anisotropic etching of polysilicon **14** occurs until the first silicon dioxide **12** is observed and is used as the etch stop.

Suitable ion implantation is then made across the entire surface of the structure. Where the ions have sufficient energy to penetrate the first silicon dioxide region **12**, they then form a first region **30** in the substrate **10**. In all other regions, they are either absorbed into the TEOS **26**, the isolation dielectric **20***a* or **20***b*, or into the silicon nitride **22**, where they have no effect. The result is shown in FIG. **2***c*-**4**.

Oxidation of the entire structure shown in FIG. **2***c*-**4** results in the exposed regions of the first polysilicon **14** being oxidized. Thus a layer of silicon dioxide layer **32** of approximately 300 Å is formed. A layer of insulating silicon dioxide is deposited over the entire structure. It should be noted that this "layer " of silicon dioxide **32**, is formed in part from regions of TEOS **26** and silicon dioxide **24**, and a "layer " **32** is shown for illustration purpose only.

Anisotropic etching of the first layer of insulating material **12**, silicon dioxide, is then performed until the substrate **10** is observed with that used as the etched stop. In the process of anisotropically etching the silicon dioxide **12**, a portion of the layer **32** will also be etched. A second polysilicon deposition step (of approximately 3000 Å) is performed depositing in the "plug" or "hole" between adjacent strips of the TEOS spacers **26**. The polysilicon material is removed from the silicon nitride **22** by a method of topographical selectivity. The preferred method is chem-mechanical polishing (CMP). The second polysilicon **34** forms ohmic contact with the first region **30** in the substrate **10**. Polysilicon **34** may be doped and used as a diffusion source to supplement or replace the impurities forming the region **30**. Polysilicon **34** may also be replaced by any suitable conductor such as tungsten, tungsten silicide, etc. The result is the structure shown in FIG. **2***d*-**4**. The structure is then oxidized forming a thin layer of silicon dioxide **36** on the second polysilicon plug **34**.

The silicon nitride **22** is then etched until the first polysilicon **14** is reached as the etch stop. Thereafter, the first polysilicon **14** is anisotropically etched until the first silicon dioxide **12** is reached as the etch stop. The formation of the "cap" **36** on the second polysilicon **34** prevents the second polysilicon **34** from being etched during this process. This is shown in FIG. **2***e*-**4**.

A thin layer of silicon dioxide **38** is then formed over the entire structure. The layer **36** is approximately 160–170 Å in thickness and can be formed by a combination of thermal oxidation and deposition. This is shown in FIG. **2***f*-**4**.

A third layer of polysilicon **40** is then deposited over the entire structure to a thickness of approximately 2000 Å. This shown in FIG. **2***g*-**4**. The third layer of polysilicon **40** can be deposited by LPCVD.

The third layer of polysilicon **40** is then anisotropically etched. The resulting structure is a plurality of spacers **40** in the row or X direction, parallel to the plug **34** in the row or X direction. The third layer of polysilicon **40** is etched until it "clears" the silicon dioxide **38** on "top" of the plug **34**. Thus, the polysilicon spacers **40** to either side of the "plug " **34** are not connected to one another. The result is the structure shown in FIG. **2***h*-**4**.

The spacers **40** are then oxidized to form a layer of silicon dioxide **42** covering all the exposed areas of the third polysilicon spacer **40**. Ion implantation can be made at this point or prior to this oxidation step to form the second regions **70**. The silicon dioxide **38** between adjacent polysilicon spacers **40** is then anisotropically etched until the substrate **10** is exposed with that used as the etch stop. A conventional contact **44** to metal **46** connection with a deposited dielectric **48** is formed to connect the second regions **70** to a common bit line **46**. The dielectric **48** may also be silicon dioxide, the same material as the layer **42**. The resulting structure is shown in FIG. **2***I*-**4**.

Referring to FIG. **2***J*-**1**, there is shown a top plan view of the resulting structure and the interconnection of the bit lines **44** to the second regions **70** and of the control lines **40** which run in the X or the row direction and finally the source lines **34** which connect to the first regions **30** within the substrate **10**. Although the source lines **34** (as should be understood by those skilled in the art, the word "source" is interchangeable with the word "drain".) makes contact with the substrate **10** in the entire row direction, i.e. contact with the active regions as well as the isolation regions, the source line **34** electrically connects only to the first regions **30** in the substrate **10**. In addition, each first region **30** to which the "source" line **34** is connected is shared between two adjacent memory cells. Similarly, each second region **70** to which the bit line **44** is connected is shared between adjacent memory cells.

The result is a plurality of non volatile memory cells of the split gate type having a floating gate **14**, a control gate **40** which is a spacer which runs along the length of the row direction connecting to the control gates of other memory cells in the same row, a source line **34** which also runs along the row direction, connecting pairs of the first terminal **30** of the memory cells in the same row direction, and a bit line **44** which runs along the column or Y direction, connecting pairs of the second terminal **70** of the memory cells in the same column direction, The formation of the control gate, the floating gate, the source line, and the bit line, are all self-aligned. The non-volatile memory cell is of the split gate type having floating gate to control gate tunnelling all as described in U.S. Pat. No. 5,572,054, whose disclosure is incorporated herein by reference with regard to the operation of such a non-volatile memory cell and an array formed thereby.

A variation of the processing of the polysilicon **40** in FIGS. **2***g*-**4** to **2***h*-**4** is as follows. When the polysilicon **40** is etched, the resulting spacers may have a rounded appearance. It is beneficial that these spacers are more of a square shape. FIG. **8** shows one embodiment of how to make polysilicon spacers with uniform dimensions. A polysilicon film **3300** (preferably 200 nm) intended to form the spacer may be conformally deposited over a mandrel **3301** which could be another gate of a sacrificial film. An oxide film **3302**, preferably 20–40 nm, may then be conformally deposited over the polysilicon film **3300**. An anisotropic etch chemistry may then be used, as shown in FIG. **9**, to remove the oxide film **3302** from the planar top surface **3400** and then to begin to remove the polysilicon film **3300**. The etch rate ratio of this etch is such that oxide **3302** on the planar surface **3400** is removed more slowly than polysilicon **3300**. Because the etch rate of any film using RIE processing is enhanced at exposed corners, the spacer **3500** projects from the corner of the polysilicon **3300** from the enhanced etch rate and preserves the vertical polysilicon **3300** etch profile as shown in FIG. **10**. Accordingly, this processing shown in FIGS. **8**-**10** may be used to form square wordline spacers **12**.

The following discussion relates to the doping of the well regions in the silicon substrate **10**, as shown in FIG. **11**. This discussion more particularly relates to implanting the first region **30** in the substrate **10**. A floating gate **3600** (along with its mirror floating gate, as discussed above) may be patterned and formed. A floating gate well **3601** is formed by subsequently implanting through the floating gate **3600**. The floating gate **3600** of the cell and its mirror cell may be separated by etching through the floating gate **3600** down to the substrate **10**. A first terminal region **3603** may then be implanted into the floating gate hole in a conventional manner. Polysilicon **3602** may then be deposited into the floating gate hole (plug to the first terminal **30**) to form a floating gate injector point. A screen oxide may be grown on the injector tip and over the wordline channel. The wordline spacer **3606** may be subsequently deposited and etched. The bitline junction **3605** and a bit line halo **3700** may then be implanted. The halo **3700** is preferably formed by implanting at an angle such that it forms under the wordline spacer **3606** and immediately next to the bitline/second terminal region **3605**.

The single well method of forming the foregoing described memory cell is advantageous because it reduces the process cost and complexity by eliminating the memory well mask, enhancing cell reliability by avoiding the need to implant into the injector tip insulator and subjecting the tip insulator to the application and removal of photoresist, and improves the manufacturability of the cell by reducing the sensitivity of the cell electrical characteristics to variations in the cell dimensions.

Referring to FIG. **3** there is shown a cross-sectional view similar to the cross sectional view shown in FIG. **1***c*-**4**. After the silicon nitride strips **22** are formed in the row direction, and the silicon dioxide **24** removed, the polysilicon **14** can then be isotropically etched to create an undercut **50**. As shown in FIG. **2***i*-**4**, and as described in the aforementioned U.S. Patent, it is desirable to have a sharp tip formed in the floating gate **14** in order to enhance the poly-to-poly tunnelling effect. The formation of the undercut **50**, as shown in FIG. **3**, through isotropic etching of the polysilicon **14** enhances the formation of the sharp tip in the eventually formed floating gate **14**.

Referring to FIG. **4***a*-**1**, there is shown a top plan view of the first step of another embodiment of the method of the present invention. The steps shown in FIGS. **4***a*-**1**, **4***a*-**2**, **4***b*-**1**, **4***b*-**2** are identical to those described for the process shown in FIGS. **1***a*-**1**, **1***a*-**2**, **1***b*-**1** and **1***b*-**2**. Similar to the foregoing description with regard to the formation of the isolation regions **20**, it is assumed that the isolation regions **20** are of the shallow trench type and the trench is planar with respect to the first polysilicon **14**.

Thus, alternating stripes of active regions and isolation regions **20** of shallow trench are formed in the substrate **10**. A second insulating layer **13** is then formed on the entire surface of the structure shown in FIG. **4***b*-**1**. This insulating layer may be formed by thermal oxidation of the first polysilicon **14**, or deposition by CVD, or a combination of these processes. It is also common in the current state of the art to form this insulator as a composite of silicon dioxide/silicon nitride/silicon dioxide (ONO). A second layer of polysilicon **15** is then deposited on the second layer of silicon dioxide or ONO **13**. The second layer of polysilicon **15** is formed by deposition (for example CVD) resulting in the second layer of silicon dioxide **13** being of about 100 Å in thickness, and the second layer of polysilicon **15** being of about 100 Å in thickness.

Thereafter, strips of silicon nitride **22** are formed in the row or X direction on the polysilicon **15**. The formation of strips of silicon nitride **22** on the polysilicon **15** is identical to the process of the formation of the silicon nitride **22** on the first polysilicon **14** as described and shown in FIG. **1***c*-**1**, **1***c*-**3** and **1***c*-**4**. Each strip of silicon nitride **22** cross over an active region and over an isolation region of shallow trench **20**, in the substrate **10**. The result is shown in FIG. **4***c*-**1**, **4***c*-**3**, and **4***c*-**4**.

Similar to the foregoing discussion with regard to the formation of the structure shown in FIG. **1** using a non self-aligned method, the structure shown in FIG. **4***c* can be formed by a non self-aligned method.

Thereafter, similar to the process described for the structure shown in FIG. **2***a*-**4**, another layer of silicon dioxide **26** is then deposited everywhere. The silicon dioxide **26** is then anisotropically etched until it "clears" the top of each of the silicon nitride strips **22**. The result is shown in FIG. **5***a*-**4**. The silicon dioxide **26** is a spacer formed in the row direction and is immediately adjacent and contiguous to each strip of silicon nitride **22**. Alternating steps of anisotropic etching are performed. First, anisotropic etching of second layer of polysilicon **15** is performed, until it reaches the second silicon dioxide **13**, which is used as the etch stop. Thereafter, anisotropic etching of the second layer of silicon dioxide **13** occurs until it reaches the first polysilicon layer **14** which is used as an etch stop. Anisotropic etching of first layer of polysilicon **14** is performed, until it reaches the first silicon dioxide **12**, which is used as the etch stop. Ion implantation into the substrate **10** is then performed forming the first region **30** in the substrate **10**. Of course, ion implantation into the substrate **10** need not occur after the etching of the second polysilicon **15**, second silicon dioxide **13**, and the first polysilicon **14**. Ion implantation can occur after any of those etch steps.

An insulator **32** is deposited over the entire structure. The insulator **32** may be silicon dioxide, silicon nitride or any other dielectric. One example is silicon dioxide which is formed as a result of direct oxidation of the second polysilicon **15** and the first polysilicon **14**. The exposed silicon dioxides **32** are anisotropically etched by RIE to expose the first region **30** while maintaining the insulation around the polysilicon **14** and polysilicon **15**. A third polysilicon **34** is deposited over the entire structure. It is removed with a topographically selective process such as CMP. This proce-

dure is the same as that used in the description of FIG. **2***d*-**4**. The third silicon **34** forms an ohmic contact to the first region **30** in the substrate **10**. The "top" of the polysilicon **34** is oxidized to form a silicon dioxide **36** cap. The result is the structure shown in FIG. **5***b*-**4**.

The silicon nitride **22** is then etched reaching the second polysilicon **15** as the etch stop. The second polysilicon **15** is then anisotropically etched reaching the second silicon dioxide **13** as the etch stop. The second silicon dioxide **13** is anisotropically etched reaching the first polysilicon **14** as the etch stop. The first polysilicon **14** is anisotropically etched reaching the first silicon dioxide **12** as the etch stop. The first silicon dioxide **12** is anisotropically etched reaching the substrate **10**. The result is the structure shown FIG. **5***c*-**4**. Thereafter, the second region **70** and bit line **46** connection to the second region **70** are formed in a conventional process. A typical sequence would involve dielectric **48** deposition followed by lithographic contact hole definition and etch followed by metal deposition and patterning, all as shown in FIG. **5***d*-**4**.

In yet another embodiment of the method of the present invention, the method begins with the process steps shown and described for the formation of the structure shown in FIGS. **1***a*-**1**, **1***a*-**2**, **1***b*-**1**, and **1***b*-**2**. After the first silicon dioxide layer **12** and first polysilicon layer **14** are formed and the isolation regions and grooves **16** are formed by the masking step, and the isolation regions of shallow trench are formed, strips of silicon nitride **22** in the row direction are then formed. Further, as described in FIG. **3**, undercutting of the first polysilicon layer **14** under the silicon nitride strip **22** can be made so as to form the undercut region **50**. Thereafter, a thin layer of silicon dioxide or ONO **26**, on the order of 120 Å thickness formed by oxidation and LPCVD process is then deposited over the entire structure. This is shown in FIG. **6***a*-**4**.

Polysilicon **34** is then deposited everywhere. This can be done by LPCVD. The result is shown in FIG. **6***b*-**4**.

Polysilicon **34** is then selectively etched by a planarizing process such as CMP using silicon nitride **22** as the etch stop. The result is the removal of all polysilicon **34** and silicon dioxide **26** from the "top" of the silicon nitride **22**. The resulting structure is shown in FIG. **6***c*-**4**.

Thereafter, the polysilicon **34** is etched at a controlled rate for a predetermined period of time such that a layer of polysilicon **34**, of approximately 500 Å thickness remains in the region between adjacent strips of silicon nitride **22**. The etch may be anisotropic (RIE) or isotropic. The result is the structure shown in FIG. **6***d*-**4**.

Silicon dioxide **36** is then deposited over the entire structure. It is then anisotropically etched and this results in the formation of spacers which are continuous in the row direction and immediately adjacent to the silicon dioxide **26** which is adjacent to the silicon nitride **22**. The result is shown in FIG. **6***e*-**4**.

Because the silicon dioxide spacers **36** are spaced apart, the polysilicon **34** is exposed and can be anisotropically etched. The polysilicon **34** is anisotropically etched until the silicon dioxide **26** is reached and is used as the etch stop. Silicon dioxide **26** is anisotropically etched (this etch also etches away some of the silicon dioxide **36**), until the first polysilicon **14** is reached and is used as the etch stop. The first polysilicon **14** is then anisotropically etched (this also results in etching of some of the polysilicon **34**), until the first silicon dioxide **12** which is used as an etch stop is reached. Ions are then implanted through the first silicon dioxide **12** to form the first region **30** in the substrate **10**. The result is shown in FIG. **6***f*-**4**. Similar to the discussion heretofore, the step of ion implantation to form the first region **30** can be made prior to the etching of the first polysilicon **14** or even prior to the etching of the silicon dioxide **26**. Silicon dioxide is then formed everywhere and in particular covering the polysilicon **34** and the first polysilicon **14**. This can be accomplished by CVD. The first silicon dioxide **12** is anisotropically etched. A source line **50** comprised of polysilicon fills in the region between the adjacent strips of silicon dioxide spacers **36**, and the silicon nitride **22** and forms an ohmic contact with the first region **30** in the substrate **10**. The result is shown in FIG. **6***g*-**4**.

Silicon nitride **22** is then etched until the first polysilicon **14** is reached which is used as an etch stop. The first polysilicon **14** is then anisotropically etched until the first silicon dioxide **12** is reached and is used as an etch stop. The silicon dioxide **12** may optimally be anisotropically etched until the substrate **30** is reached with the substrate **10** being used as an etch stop. The result is the structure shown in FIG. **6***h*-**4**.

Thereafter, the formation of the control gate spacer **40** and of the second region **70** are all as shown and described above for FIGS. **2***f*-**4**–**2***i*-**4**. The result is the structure shown in FIG. **6***i*-**4**.

The difference between the non-volatile memory cell shown in FIG. **6***i*-**4** and the non-volatile memory cell shown in FIG. **2***i*-**4** is the addition of a second control gate **34**. The second control gate **34** which is also parallel to the control gate **40** and to the source line **50**, offers the ability to apply a different positive or negative voltage to capacitively couple to the floating gate **14** to enhance performance during various read or write. As a special case, the second control gate **34** can also be electrically connected to the source line **50** to provide greater capacitive coupling between the first region **30** and the floating gate **14**.

The foregoing has described three self aligned methods to form non-volatile memory cell arrays of the floating gate memory cell type. By use of spacers to define the gate lengths, a uniform array of gates whose dimension is not limited by lithographic capability may be realized. In addition, by using polysilicon (or conductive) lines to connect to the first and second regions in the substrate (as opposed to source or drain lines in the substrate itself), the methods have provided for a unique manner to interconnect to semiconductor circuits, such as memory cells of any type, arranged in an array.

Referring to FIG. **7***a*-**4**, there is shown a cross sectional view taken along the line **4**—**4** showing the result of processing in which the structures **90** shown in FIG. **2***e*-**4**, **5***c*-**4**, or **6***h*-**4** are formed. Although the starting structure of FIG. **7***a*-**4** is the result of the processing shown in FIG. **2***e*-**4**, **5***c*-**4**, or **6***h*-**4**, it should be noted that it is not necessary that the structure **90** be formed by the methods described and leading to that shown in FIG. **2***e*-**4**, **5***c*-**4**, or **6***h*-**4**. It is only necessary that the structures **90** be spaced apart, substantially rectilinear, and have two vertical edges **92**, with a "trench" between the structures **90**. Further, the structures **90** need not be limited to non-volatile memory cells. For example, DRAM cells, SRAM cells or even logic cells that are arranged in an array of rows and columns, with word lines and bit lines to access each element **90** can be used as the starting point.

Furthermore, it is assumed that the structure **90** shown in FIG. **7***a*-**4** is of the type not having a word line within the structure **90**, such as the structure **90** shown in FIG. **2***e*-**4**. (Where a word line is within the structure **90**, such as the

embodiment **90** shown in FIG. **5***c*-**4** or **6***h*-**4**, this will be discussed hereinafter.)

The structure **90** is then either oxidized or insulating material **92** is deposited so as to surround the structure **90**. This can be done by the process shown and described in FIG. **2***f*-**4**. Of course if it is desired to electrically connect the structure **90** to the to-be-formed word lines, then this step may be eliminated.

A conductive gate material **40**, such as polysilicon is deposited everywhere including the "trench" region, i.e. the region between the vertical walls **92** of adjacent structures **90**. The polysilicon **40** is deposited by LPCVD. The polysilicon **40** will eventually form the word lines to the structures **90**.

The polysilicon **40** is selectively removed with a topographically sensitive etch so as to leave polysilicon **40** recessed, in the "trench" region only. This can be done by a combination of CMP and RIE. As will be seen, the depth of the recess in the "trench" region is such that it allows the formation of spacers. The resultant structure is shown in FIG. **7***b*-**4**.

The polysilicon **40** may now be optionally metallized, i.e. silicide may be formed on the polysilicon **40**. As is well known in the art the formation of silicide improves the electrical conductivity of the polysilicon **40**. Since silicide processes have difficulty forming in narrow polysilicon lines, forming a silicide at this point in the process is easier than later when the row lines are at their final, narrow width.

A dielectric material **82**, such as silicon dioxide, is conformally deposited everywhere, using e.g. CVD process. The resultant structure is shown in FIG. **7***c*-**4**.

The silicon dioxide **82** is anisotropically etched resulting in the structure shown in FIG. **7***d*-**4**.

The polysilicon **40** is then etched using the silicon dioxide **82** as a "hard mask". Ion implantation is then performed through the layer **12** to form the second region **70**. The resultant structure is shown in FIG. **7***e*-**4**.

The structure shown in FIG. **7***e*-**4** can further be processed by one of two methods: self-aligned and non self-aligned.

For the self aligned process, the structure shown in FIG. **7***e*-**4** is then oxidized, so that the exposed regions of the polysilicon **40** form silicon dioxide **84**. The structure is then anisotropically etched until the substrate **10** is exposed. It should be noted that in the preferred embodiment, layer **82**, **84** and **12** are all of the same material, namely silicon dioxide. A bit line plug **46** connects the bit line **46** to the second region **70**. The resultant structure is shown in FIG. **7***f*-**4**. Thus the structure shown in FIG. **7***f*-**4** is a self-aligned bit line structure, which is self aligned with respect to the structure elements **90**, with word lines **40** being formed of substantially rectilinear lines perpendicular to the bit lines **46**.

For the non self-aligned method, which is conventional and is well known in the prior art, another layer of insulation is deposited over the structure shown in FIG. **7***e*-**4**. A hole is then created using a lithographic process through this insulation to the second region of the substrate **10**. The hole is then filled with metal or conductor to form a contact with the second region **70**.

As previously discussed, the structure **90** may or may not contain word lines within the structure **90**. In the event the structure **90** contains word lines **40**, such as the structures shown in FIG. **5***c*-**4** or **6***h*-**4**, then it is not necessary to form the polysilicon lines **40**, as shown and described for FIG. **7***b*-**4**. The polysilicon **40** may be replaced by a dielectric material similar or identical to the insulator **82**, which is eventually deposited thereon. Alternatively, the insulator **82** may be conformally deposited everywhere, and then anisotropically etched to form the resultant structure shown in FIG. **7***e*-**4**.

Although the foregoing method described the use of polysilicon, it should be clear to those having ordinary skill in the art that any conductive material can be used. In addition, any insulator can be used in place of silicon dioxide. Finally, any material whose etch property differs from silicon dioxide (or any insulator) and from polysilicon (or any conductor) can be used in place of silicon nitride.

What is claimed is:

1. A self-aligned method of forming a semiconductor memory array of memory cells in a semiconductor substrate, each memory cell including a floating gate having a sharp tip, said method including the steps of:

forming a plurality of spaced apart isolation regions on said substrate, substantially parallel to one another in a first direction with an active region between each pair of adjacent isolation regions, each of said active regions comprising a first layer of insulating material on said semiconductor substrate, and a first layer of conductive material on said first layer of insulating material;

forming a plurality of spaced apart masking regions of a masking material substantially parallel to one another in a second direction on said active regions and said isolation regions, said second direction being substantially perpendicular to said first direction;

forming undercuts below said masking material along said second direction;

forming a plurality of spaced apart first spacers of an insulating material, substantially parallel to one another in said second direction, each first spacer being adjacent and contiguous to one of said masking regions with a first region between each pair of adjacent first spacers, each first spacer crossing a plurality of alternating active and isolation regions;

etching between pairs of first spacers in said first region, and through said conductive material;

removing said masking material; and

anisotropically etching said conductive material, effective to form a plurality of spaced apart floating gates, each of said floating gates having a sharp tip.

2. The method of claim **1** further comprising the step of:

forming a plurality of control gates spaced apart from said floating gates.

3. The method of claim **2** wherein said conductive material comprises polysilicon.

4. The method of claim **2** wherein said undercuts are formed by isotropically etching said conductive material.

5. The method of claim **3** further comprising the steps of:

forming a plurality of first implant regions by ion implantation, each of said first implant regions being partially overlapped by a unique one of said floating gates; and

forming a plurality of second implant regions by ion implantation, spaced apart from said first implant regions, each of said second implant regions being partially overlapped by a unique one of said control gates.

6. The method of claim **5** further comprising the steps of:

forming a first terminal in each of said first implant regions between pairs of adjacent first spacers; and

forming a conductor in said second direction between each of said pairs of first spacers, electrically connecting each of said first terminals.

7. The method of claim **6** further comprising the steps of:

forming a second terminal in each of said second implant regions; and

forming a conductor in said first direction, electrically connecting each of said second terminals.

8. The method of claim **3** wherein said control gates comprise a plurality of spaced apart second spacers of a conductive material, which are disposed in said second direction.

9. The method of claim **8** wherein said conductive material comprises polysilicon.

10. A self-aligned method of forming a semiconductor memory array of memory cells in a semiconductor substrate, each memory cell including a floating gate and a control gate, said method including the steps of:

forming a plurality of spaced apart isolation regions on said substrate, substantially parallel to one another in a first direction with an active region between each pair of adjacent isolation regions, each of said active regions comprising a first layer of insulating material on said semiconductor substrate, and a first layer of polysilicon material on said first layer of insulating material;

forming a plurality of spaced apart masking regions of a masking material substantially parallel to one another in a second direction on said active regions and said isolation regions, said second direction being substantially perpendicular to said first direction;

depositing a second layer of insulating material over said active and isolation regions;

depositing a second layer of conductive material over said second layer of insulating material;

etching said second layer of conductive material and said second layer of said insulating material using said masking material as an etch stop;

etching said second layer of conductive material between said masking regions until a predetermined thickness of said conductive material remains;

forming a plurality of spaced apart first spacers of an insulating material, substantially parallel to one another in said second direction, each first spacer being adjacent to one of said masking regions with a first region between each pair of adjacent first spacers, each first spacer crossing a plurality of alternating active and isolation regions;

etching between pairs of first spacers in said first region, and through said first and second layer of conductive material, and said first and second layer of insulating material;

removing said masking material; and

anisotropically etching said conductive material, effective to form a plurality of spaced apart floating gates, and a plurality of control gates.

11. The method of claim **10** further comprising the step of forming an undercut below each side of said masking material along said second direction, before depositing a second layer of insulating material over said active and isolation regions, said undercuts being effective to cause said floating gates to be formed with a sharp tip.

12. The method of claim **11** wherein said undercuts are formed by isotropically etching said conductive material.

13. The method of claim **10** further comprising the step of:

forming a plurality of third gates spaced apart from said floating gates.

14. The method of claim **13** wherein said third gates each comprise first control gates, and said control gates each comprise second control gates for applying a different voltage to capacitively couple to said floating gates during read and write operations.

15. The method of claim **14** further comprising the steps of:

forming a plurality of first implant regions by ion implantation, each of said first implant regions being partially overlapped by a unique one of said floating gates; and

forming a plurality of second implant regions by ion implantation, spaced apart from said first implant regions, each of said second implant regions being partially overlapped by a unique one of said first control gates.

16. The method of claim **15** further comprising the steps of:

forming a source line which is in ohmic contact with each of said first implant regions.

17. The method of claim **16** further comprising the step of electrically connecting said control gates to said source line.

18. The method of claim **13** wherein said third gates comprise a plurality of spaced apart second spacers of a conductive material, which are disposed in said second direction.

19. The method of claim **10** wherein said conductive material comprises polysilicon.

* * * * *

EXHIBIT B

US006743674B2

(12) **United States Patent**
Wang

(10) **Patent No.: US 6,743,674 B2**
(45) **Date of Patent: Jun. 1, 2004**

(54) **METHOD OF FORMING A SEMICONDUCTOR ARRAY OF FLOATING GATE MEMORY CELLS AND STRAP REGIONS, AND A MEMORY ARRAY AND STRAP REGIONS MADE THEREBY**

(75) Inventor: **Chih Hsin Wang**, San Jose, CA (US)

(73) Assignee: **Silicon Storage Technology, Inc.**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/205,289**

(22) Filed: **Jul. 24, 2002**

(65) **Prior Publication Data**

US 2003/0053347 A1 Mar. 20, 2003

Related U.S. Application Data

(60) Provisional application No. 60/323,445, filed on Sep. 18, 2001.

(51) **Int. Cl.**[7] **H01L 21/336**
(52) **U.S. Cl.** **438/257**; 438/258
(58) **Field of Search** 438/257, 258

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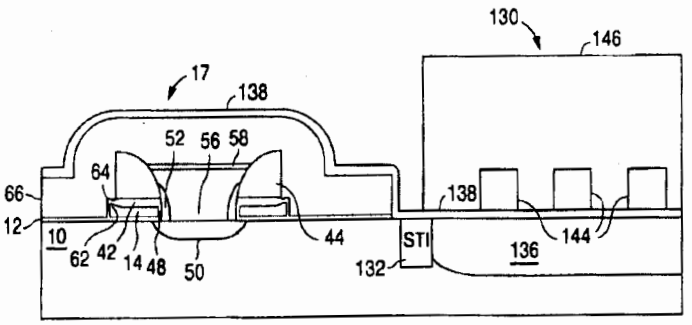
Primary Examiner—David Nelms
Assistant Examiner—Thao P. Le
(74) *Attorney, Agent, or Firm*—Gray Cary Ware & Freidenrich LLP

(57) **ABSTRACT**

A self aligned method of forming a semiconductor memory array of floating gate memory cells in a semiconductor substrate, along with strap regions interlaced within the array. The array includes word lines and source lines that connect together control gates and source regions from memory cells contained in row within the array. The strap regions include word line strap cells through which the word lines traverse, wherein the word lines completely traverse across the strap regions, and source line strap cells in which the source lines terminate without completely traversing across the strap region. The control gate polysilicon is formed over the substrate, and protected by a layer of protective material, before the formation of other polysilicon elements associated with the memory array, to ensure the proper remove of residual polysilicon stringers.

10 Claims, 30 Drawing Sheets



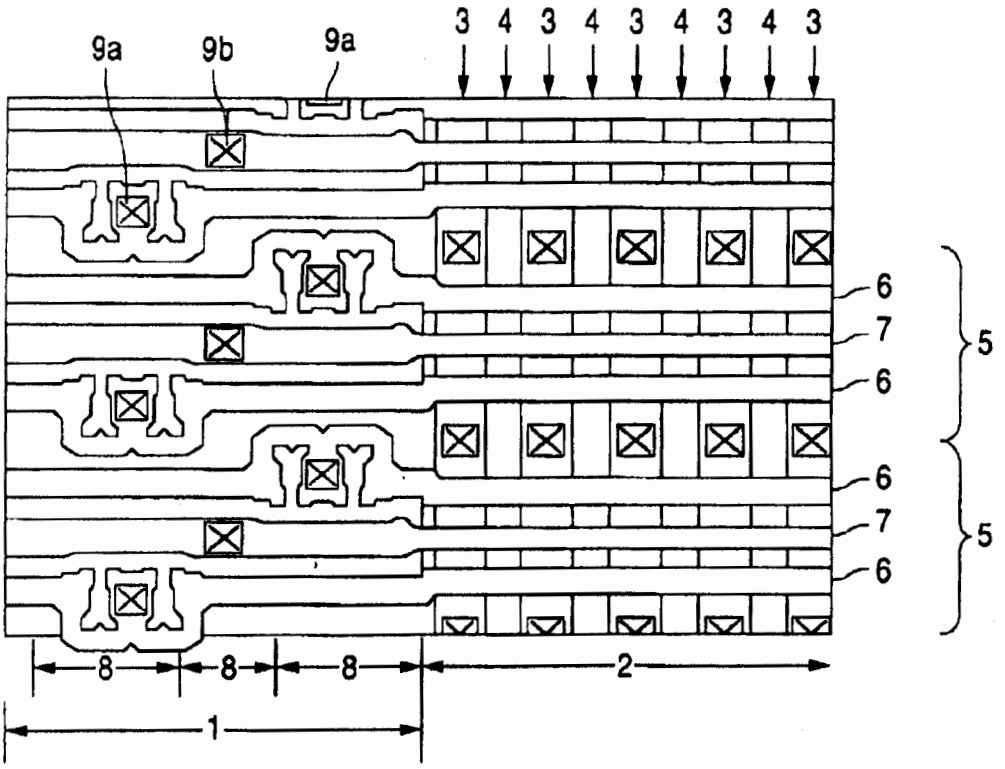

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FIG. 1

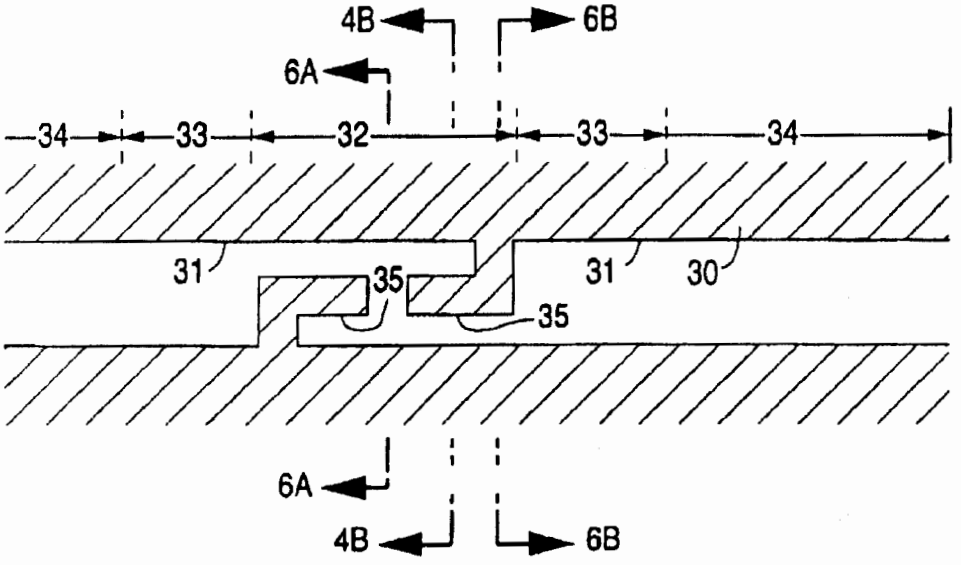
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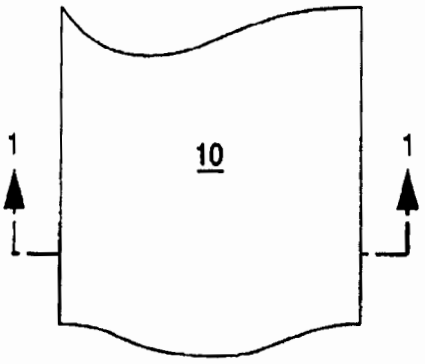
FIG. 5



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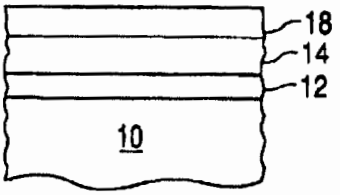

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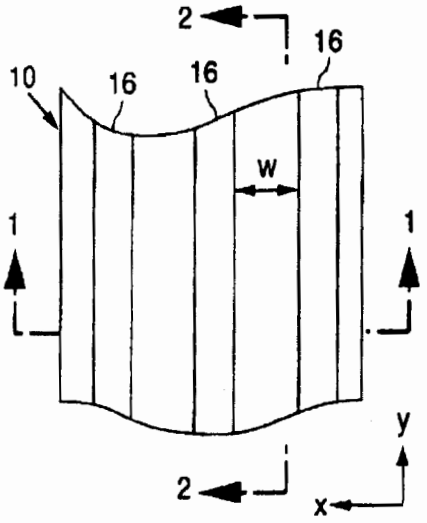

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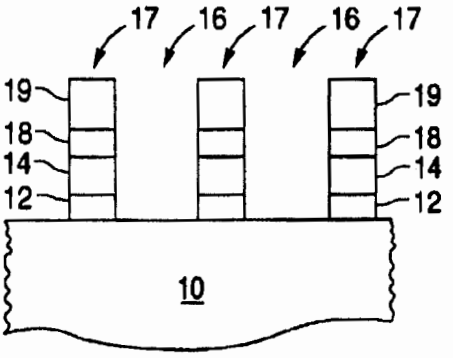


FIG. 2D

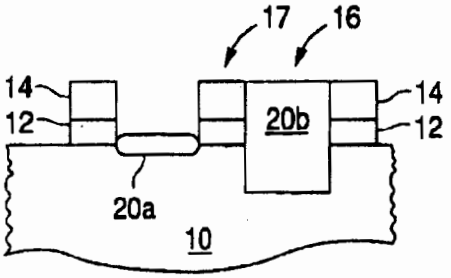


FIG. 2E

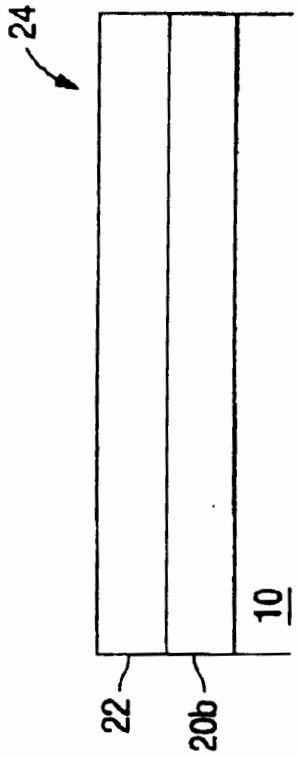
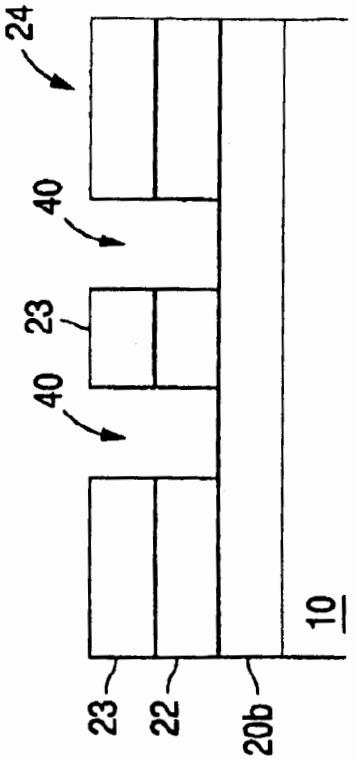


FIG. 4A



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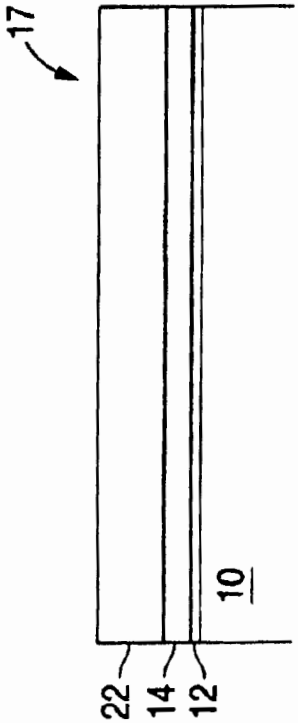

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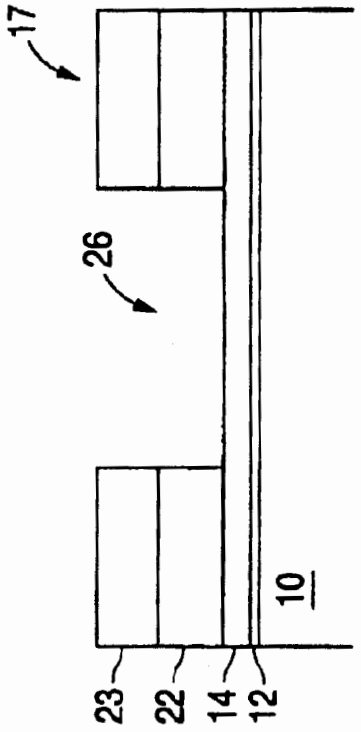

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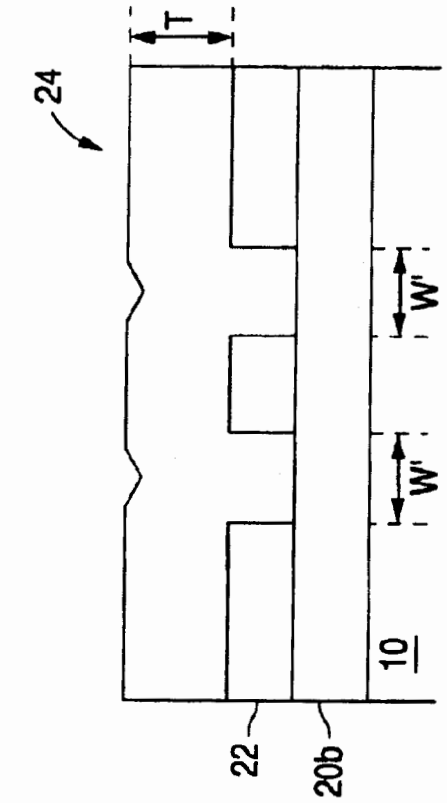

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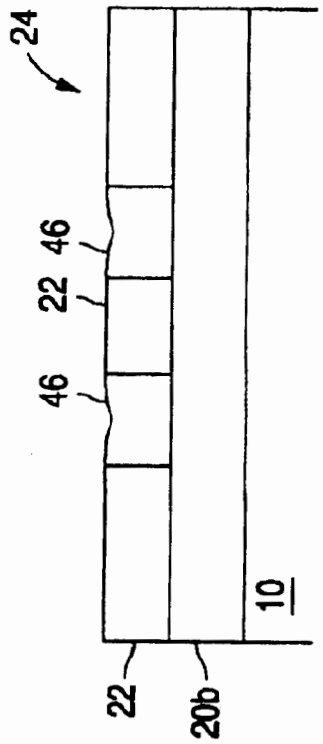

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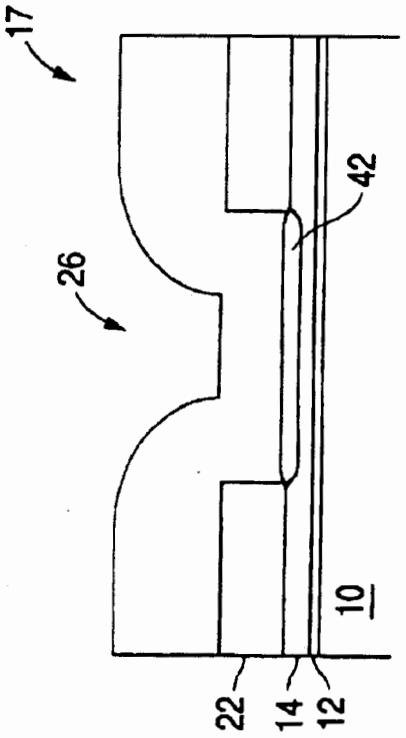

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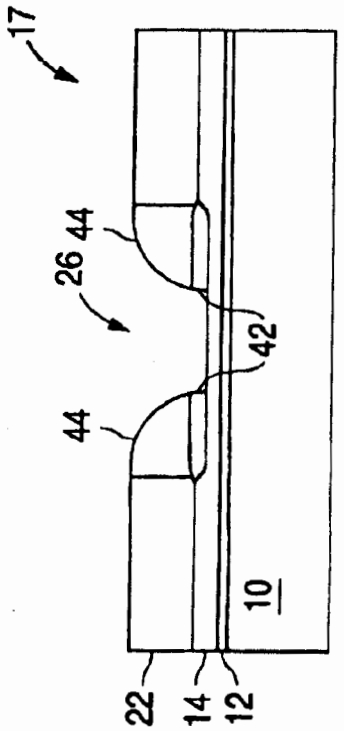

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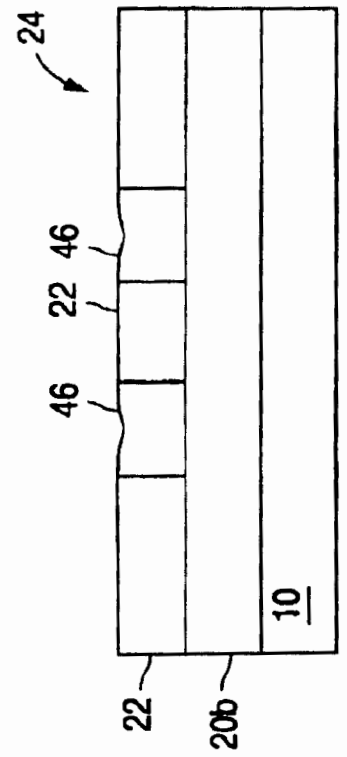

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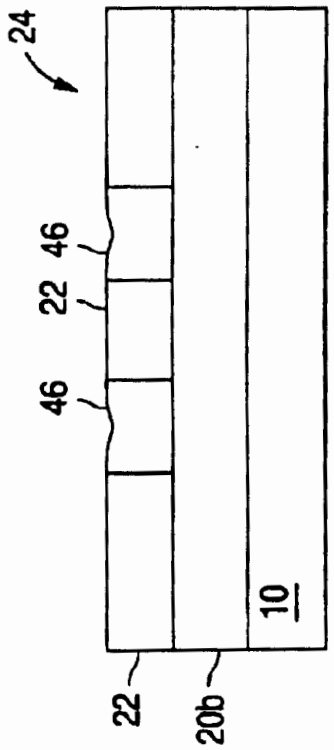

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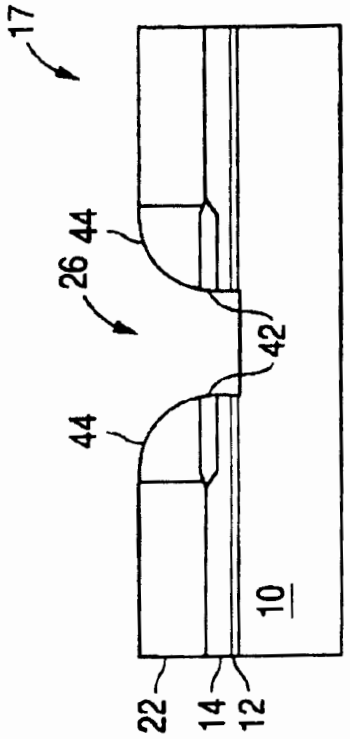

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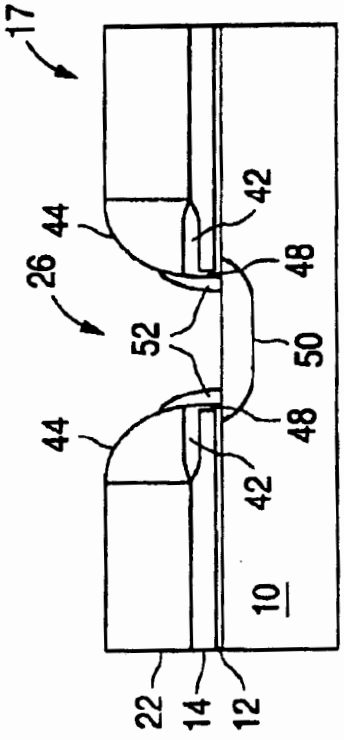

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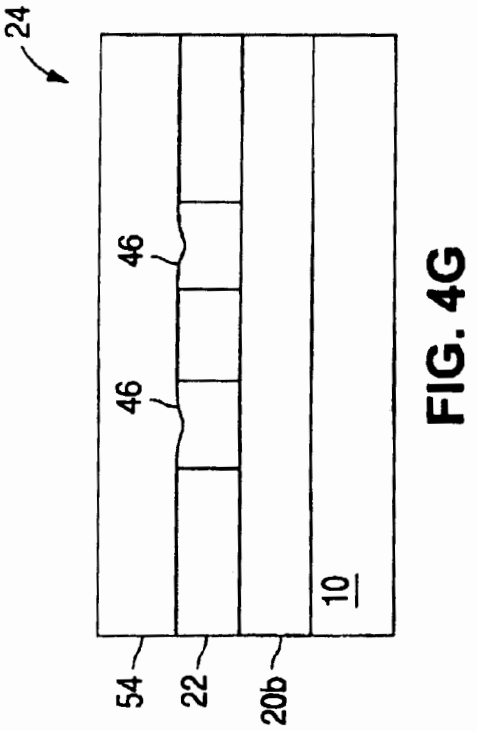

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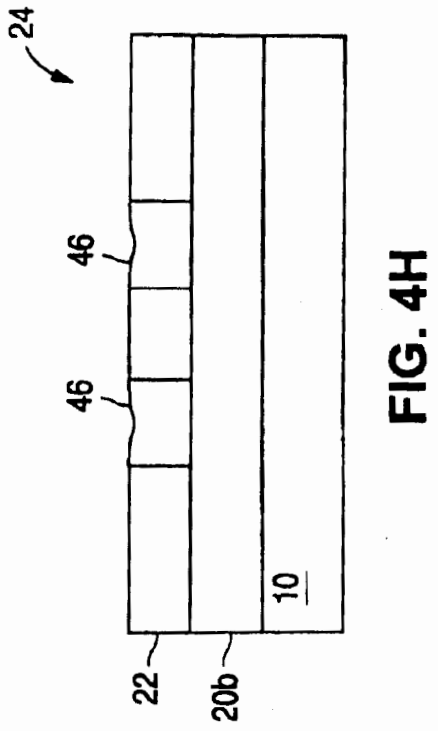

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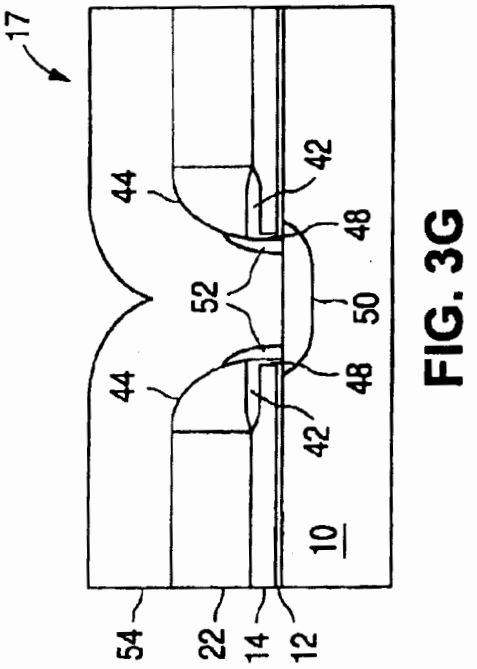

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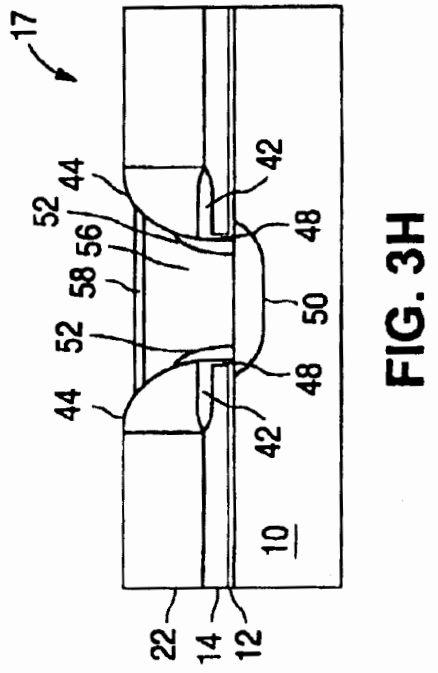

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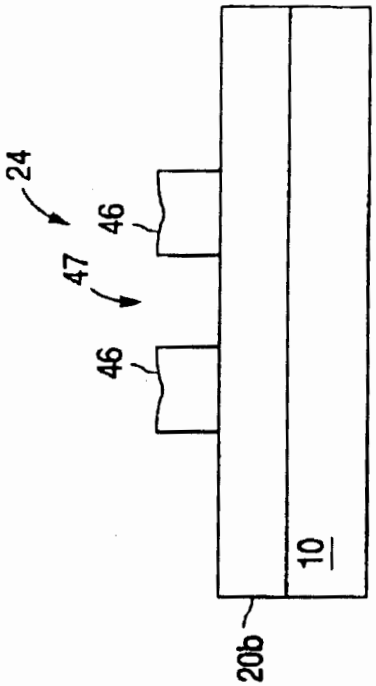
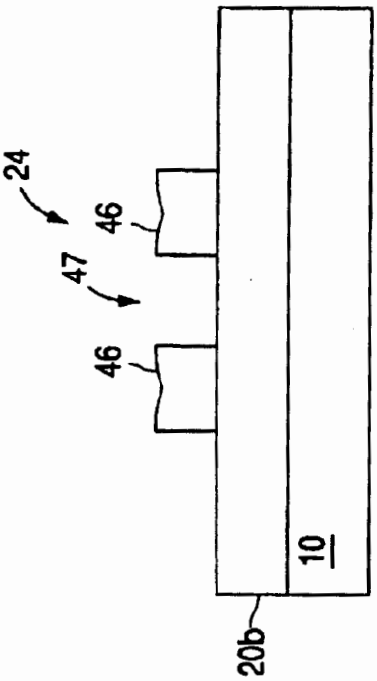


FIG. 4I



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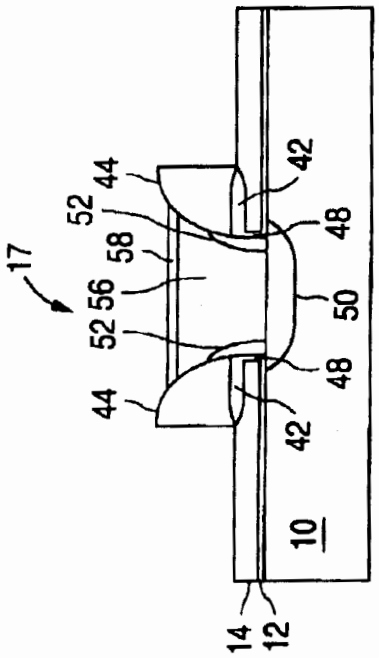

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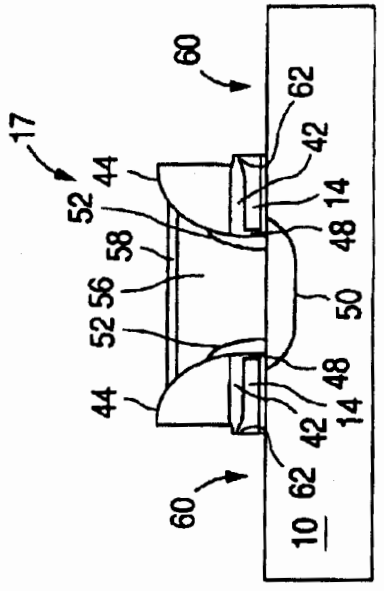

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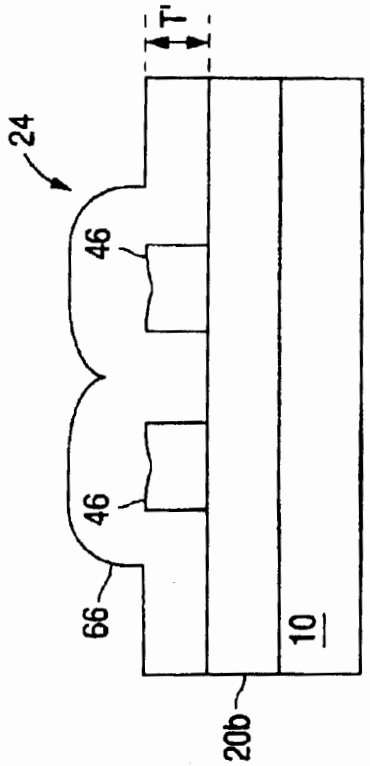

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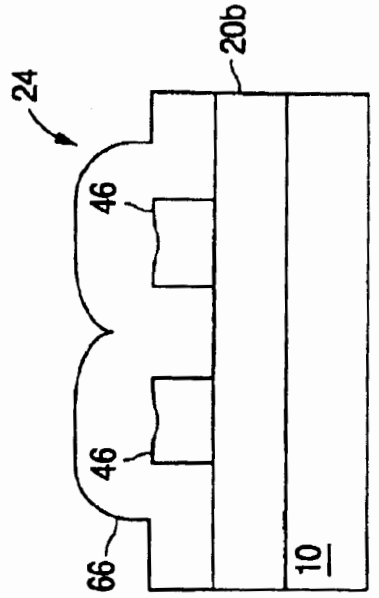

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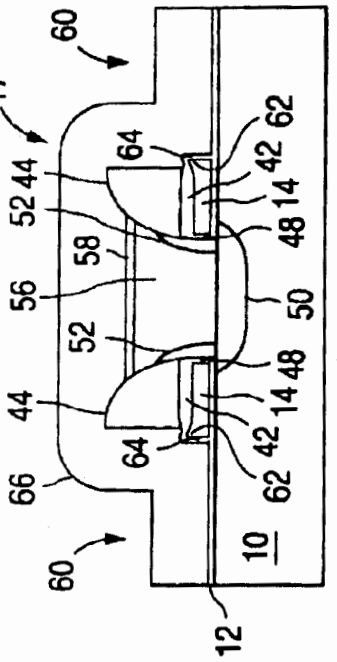

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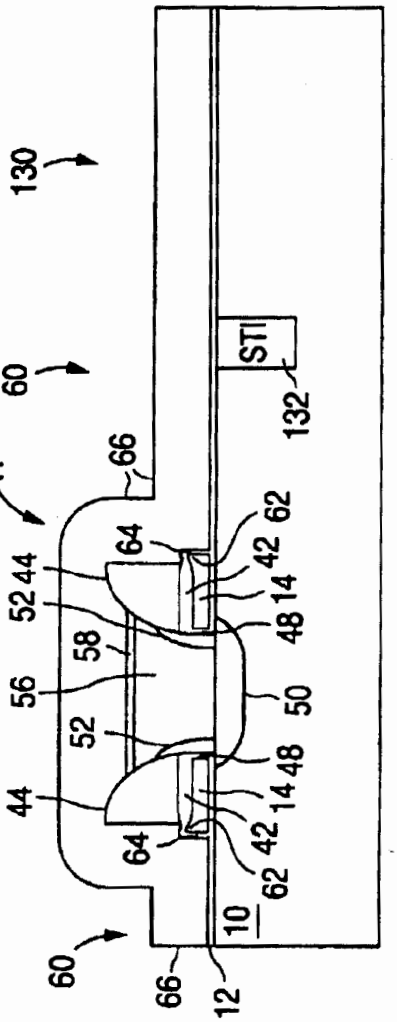

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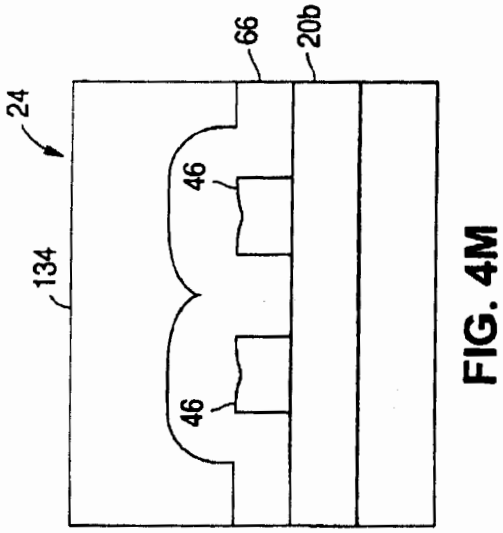

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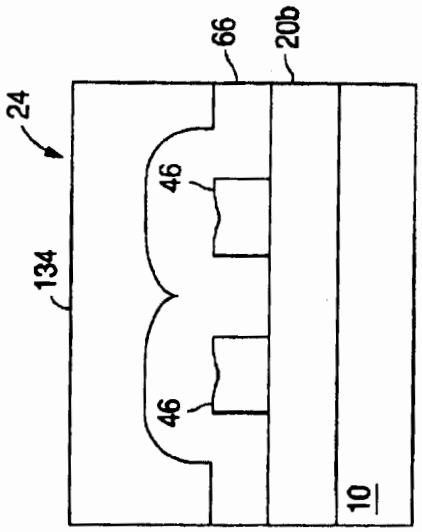

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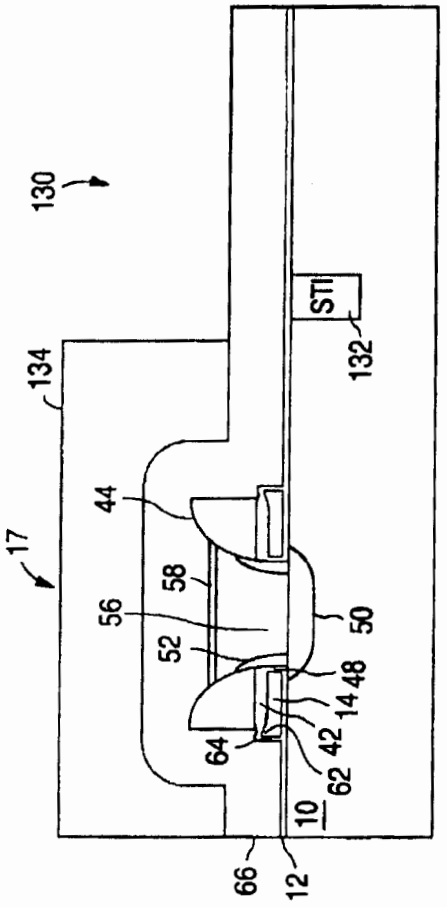

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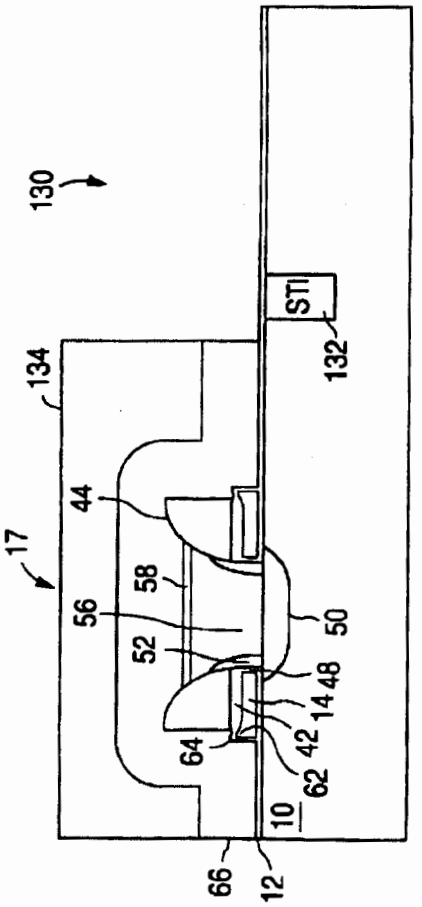


FIG. 3N

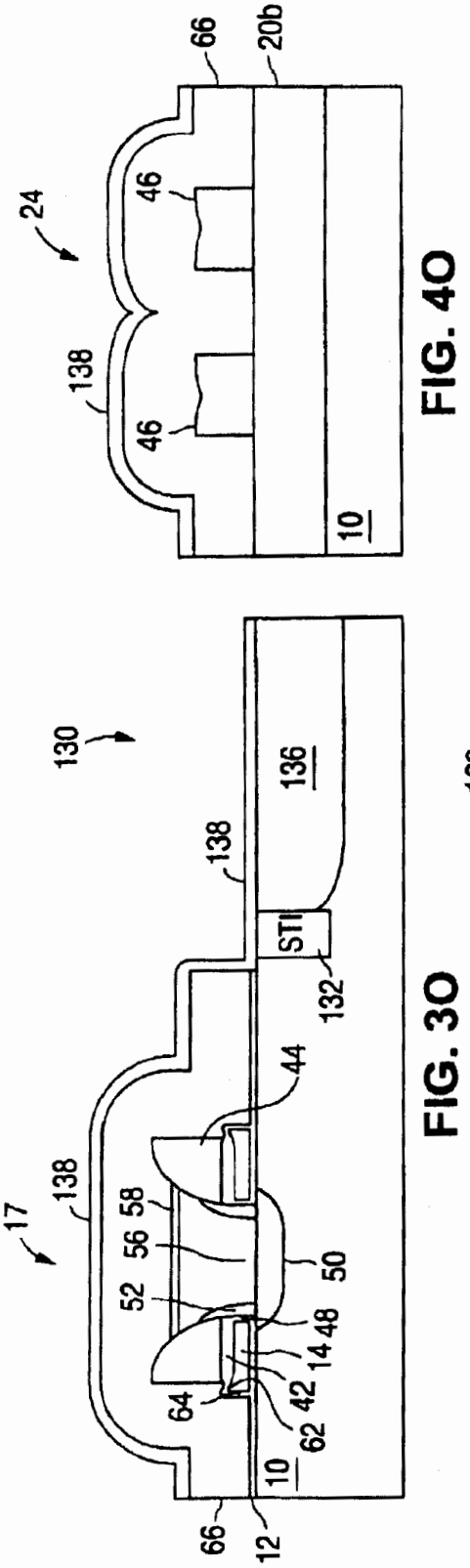
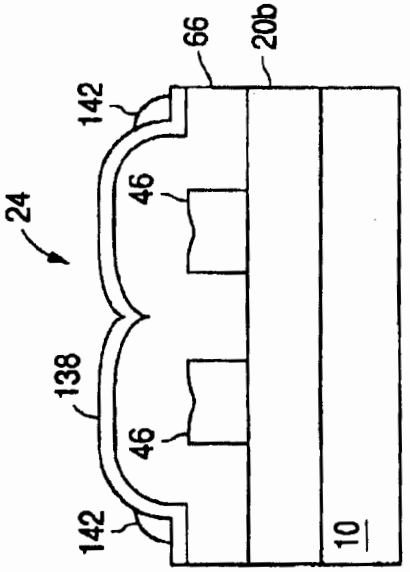


FIG. 4O

FIG. 3O



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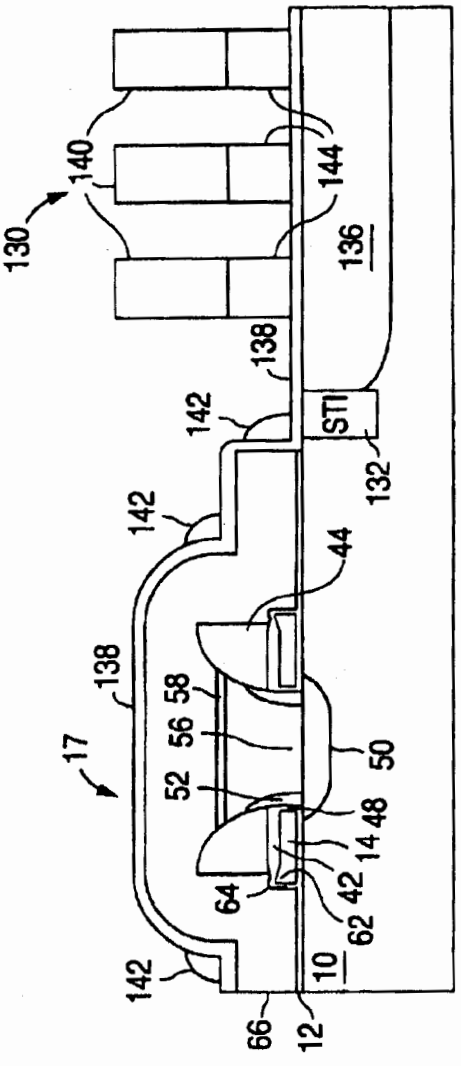

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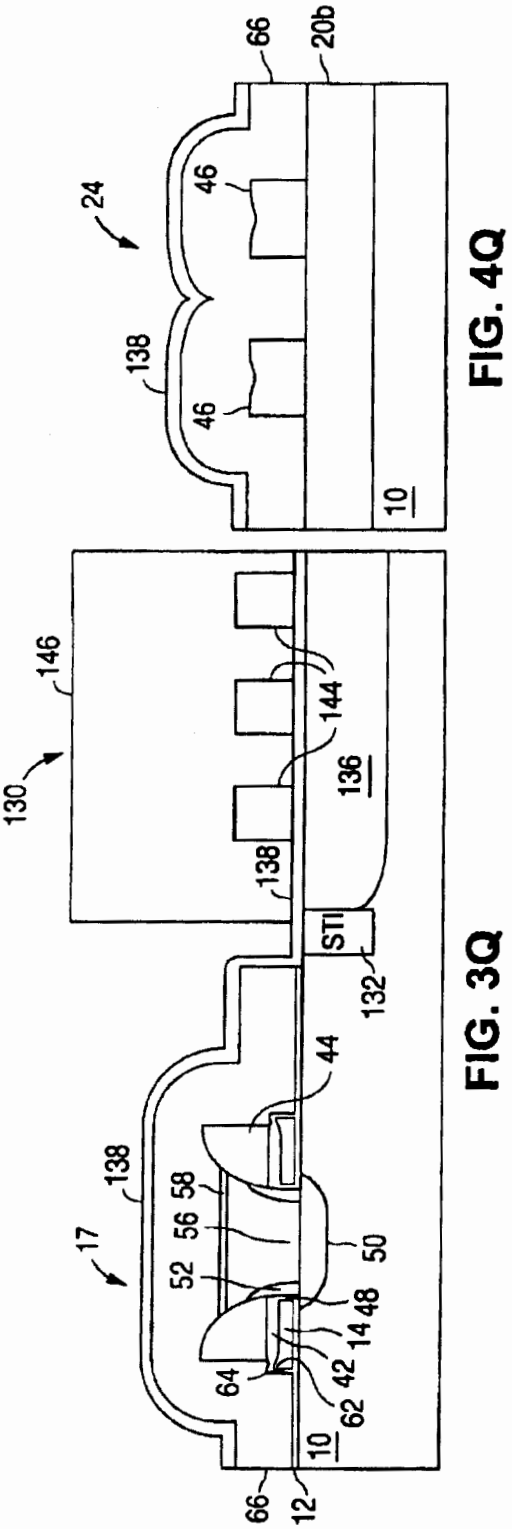


FIG. 4Q

FIG. 3Q

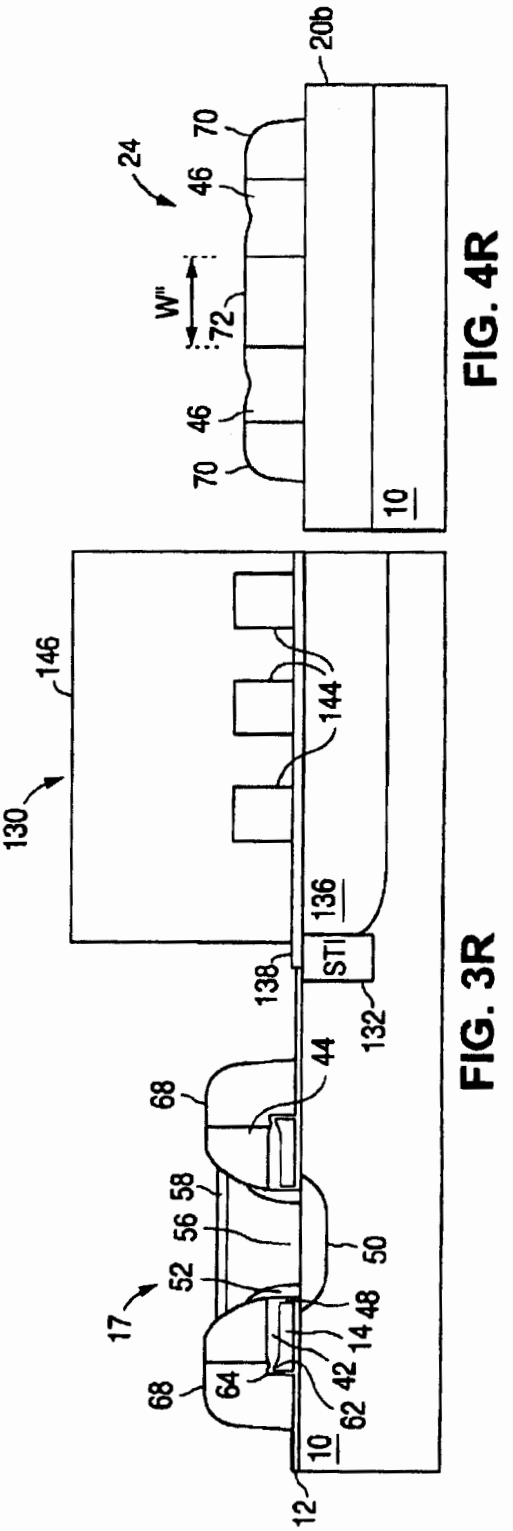
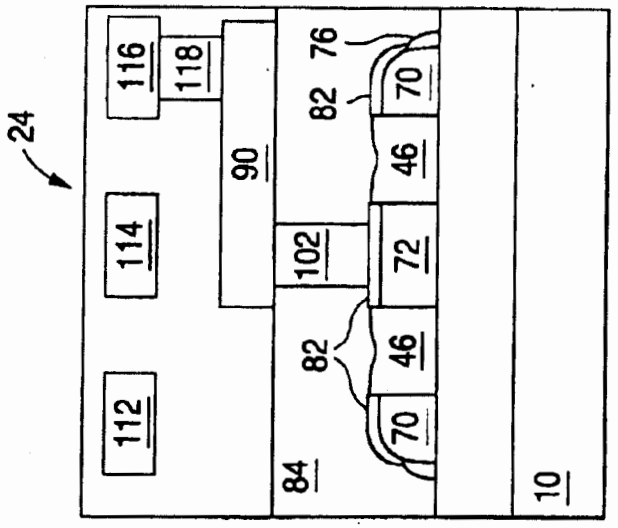


FIG. 4R

FIG. 3R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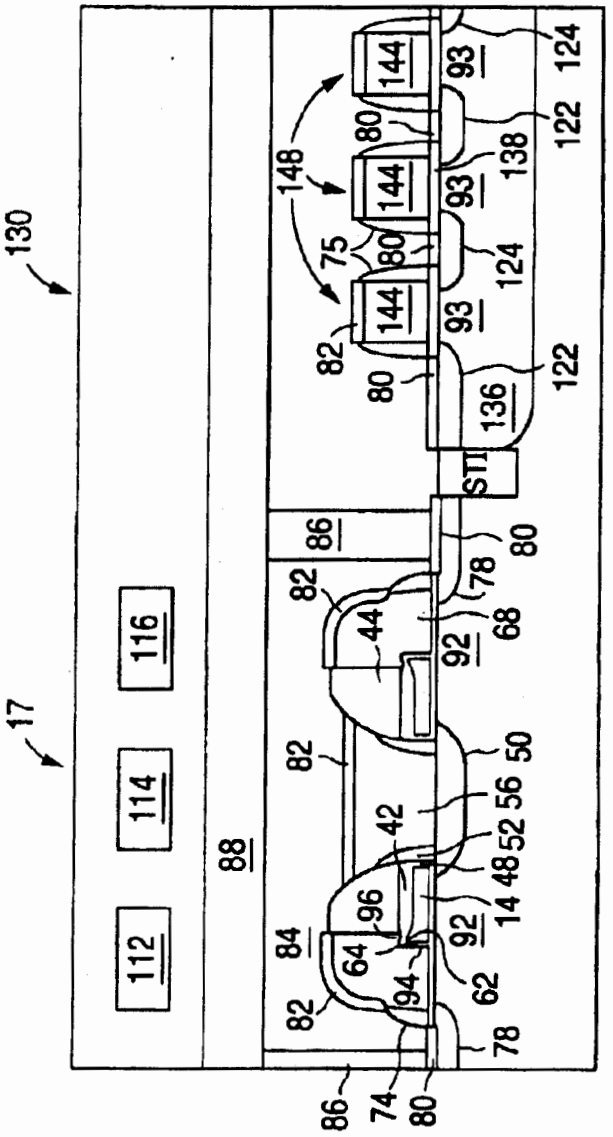
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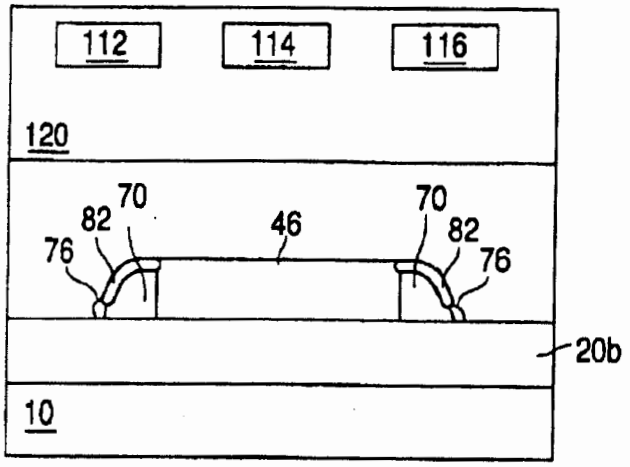
FIG. 3S



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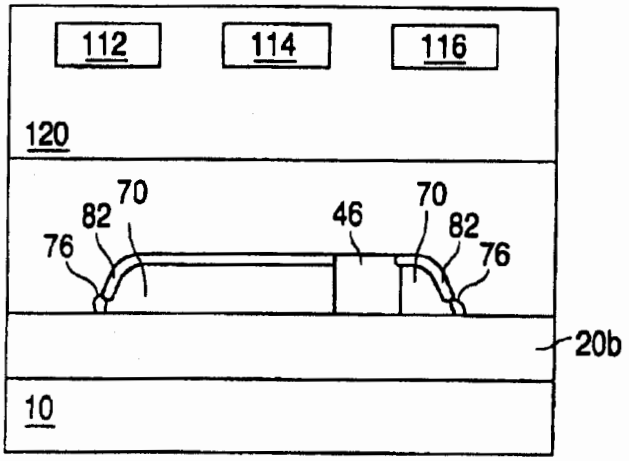

FIG. 6B

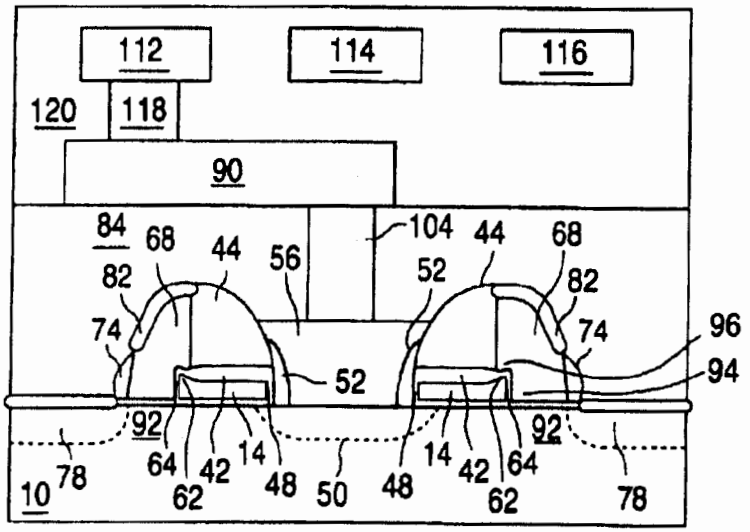

FIG. 6C

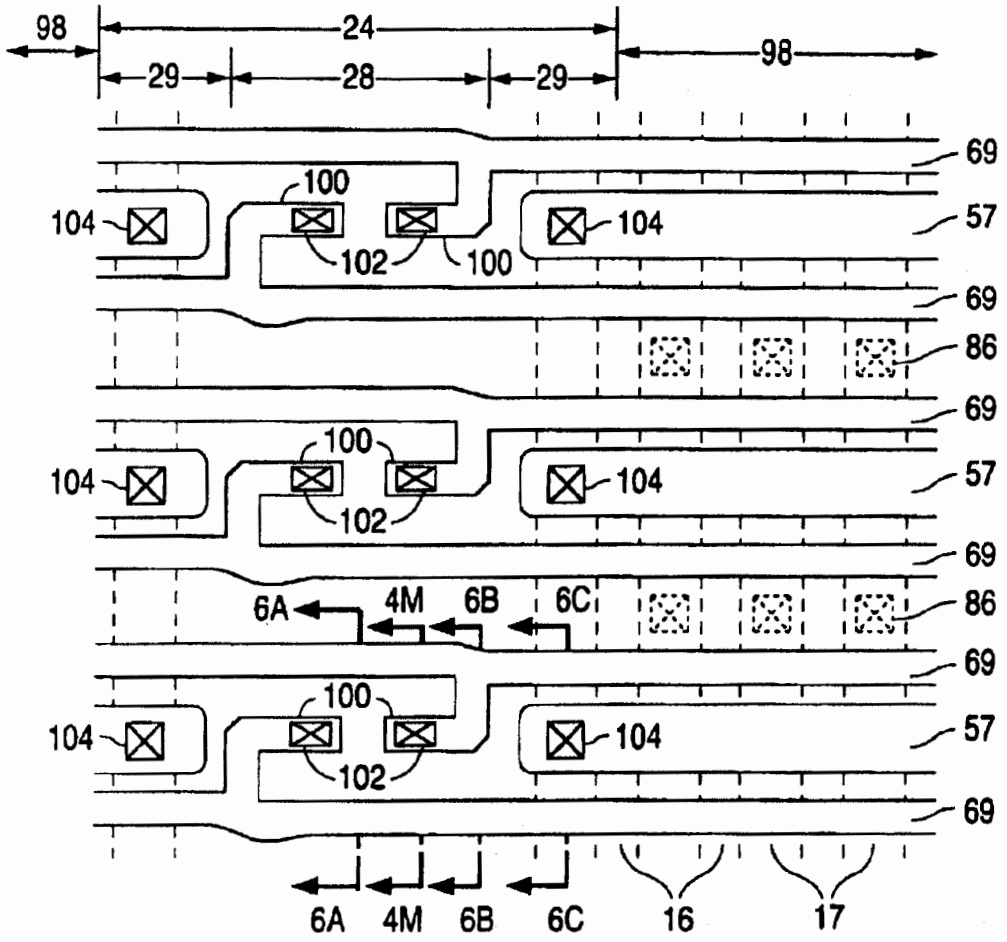
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FIG. 7

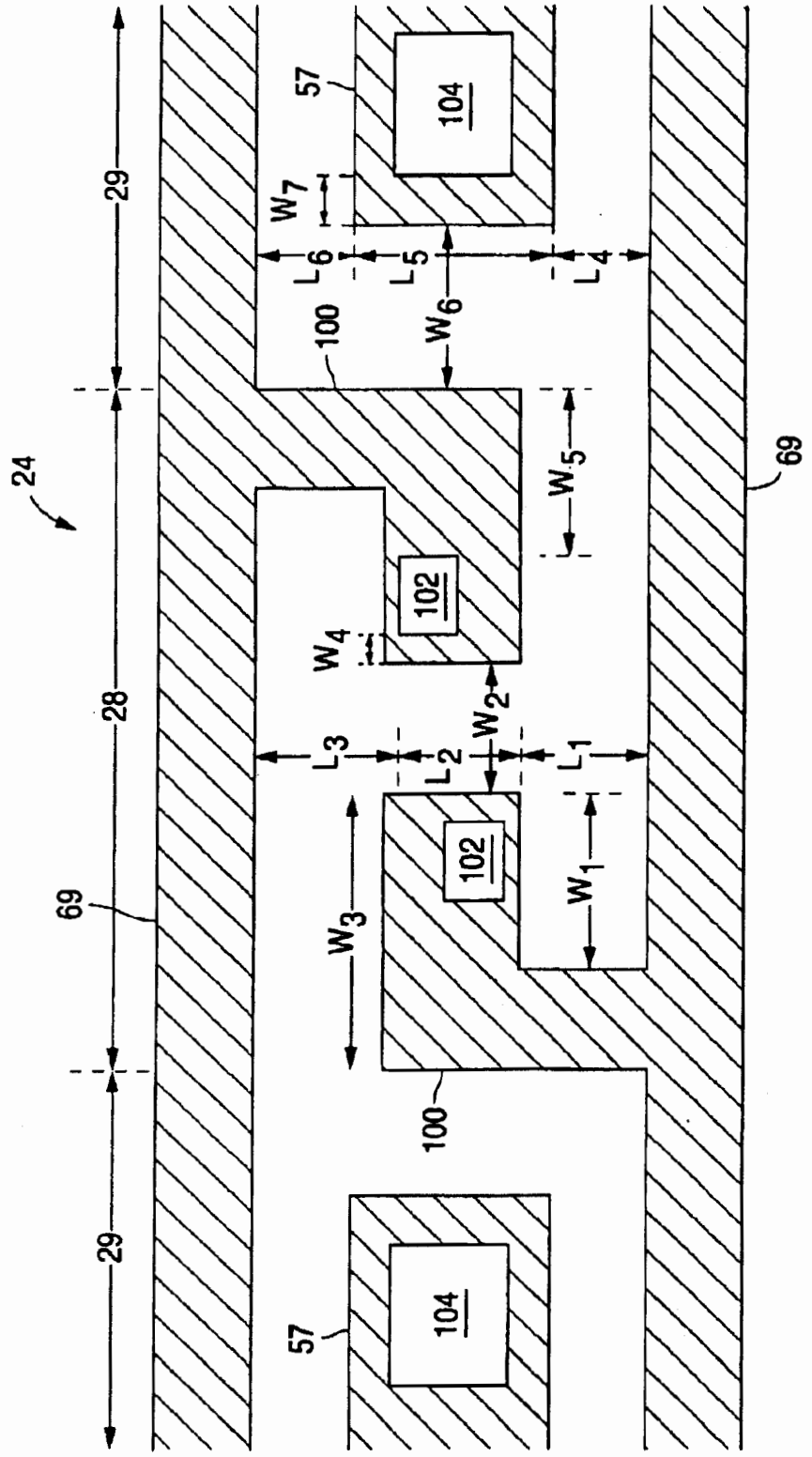
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FIG. 8

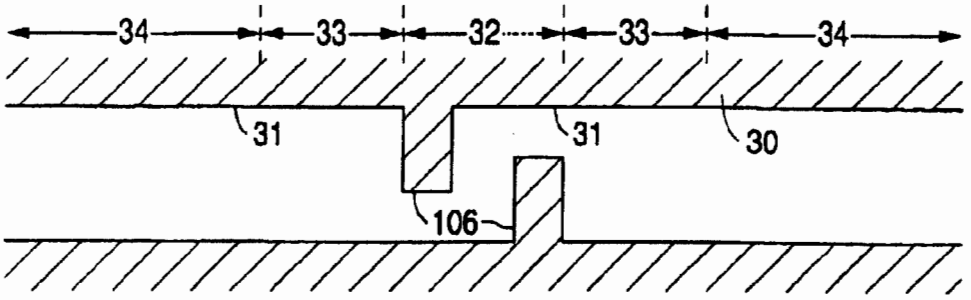

FIG. 9A

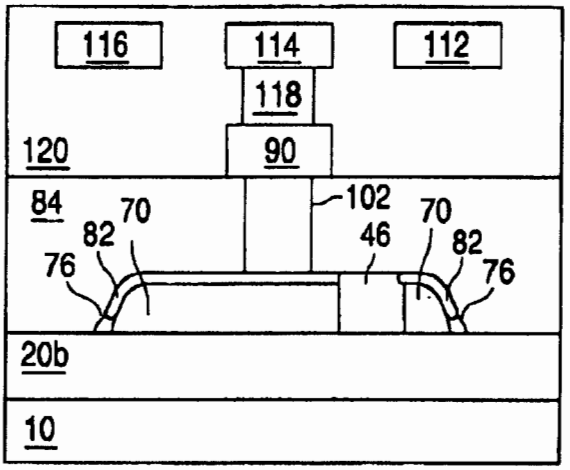

FIG. 9B

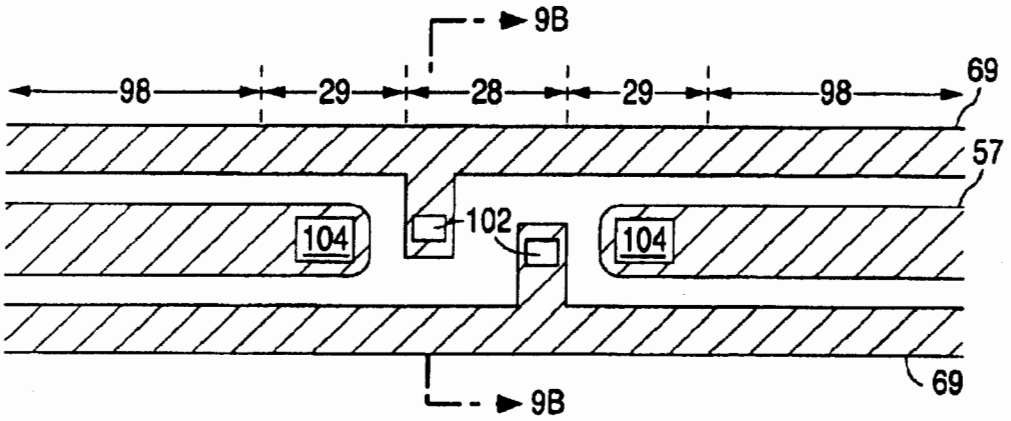

FIG. 9C

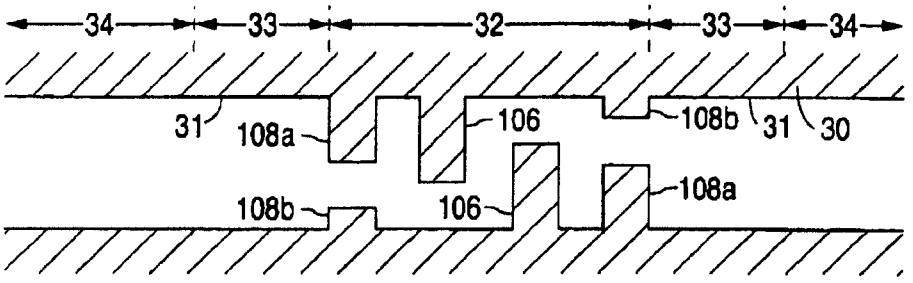

FIG. 10A

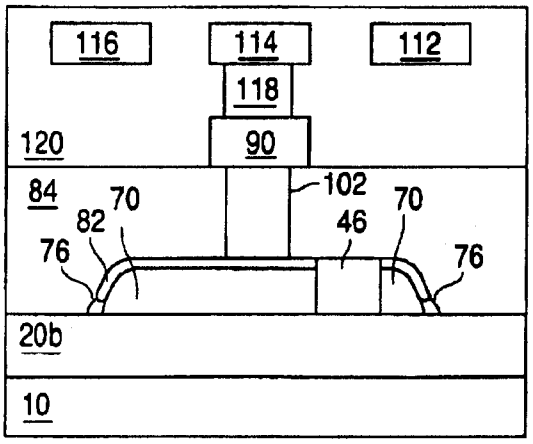

FIG. 10B

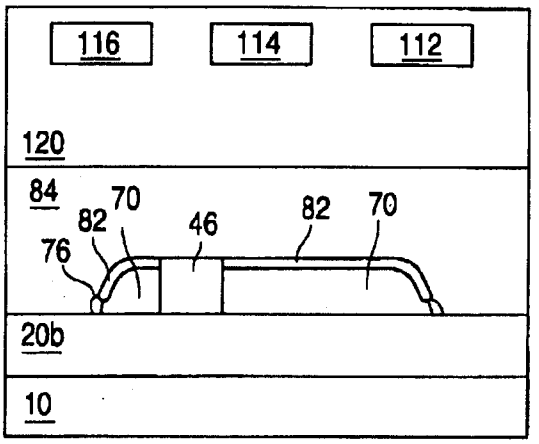

FIG. 10C

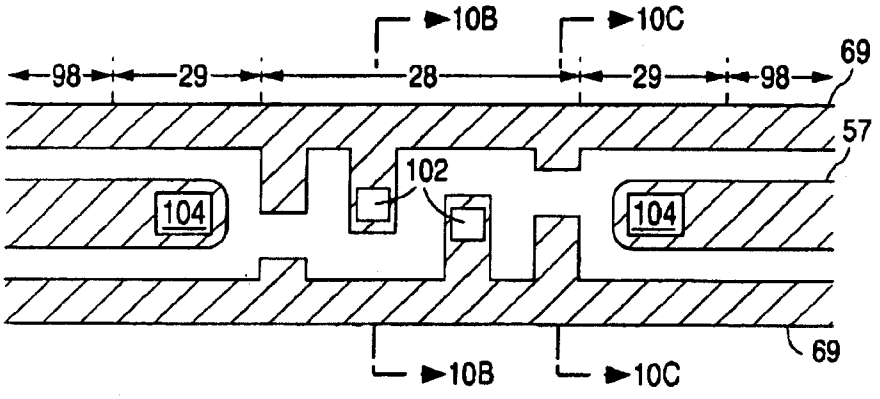

FIG. 10D

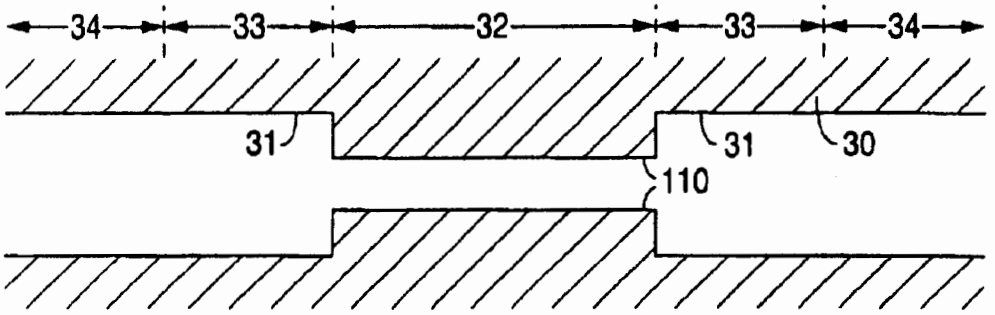

FIG. 11A

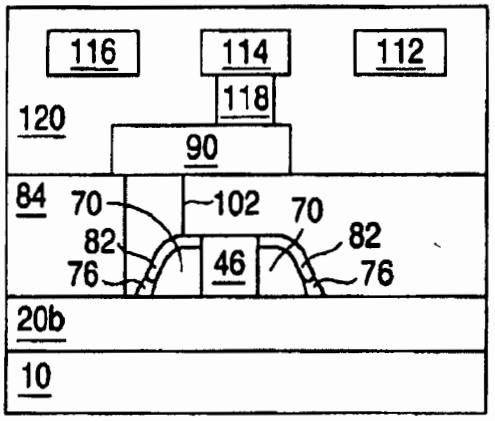

FIG. 11B

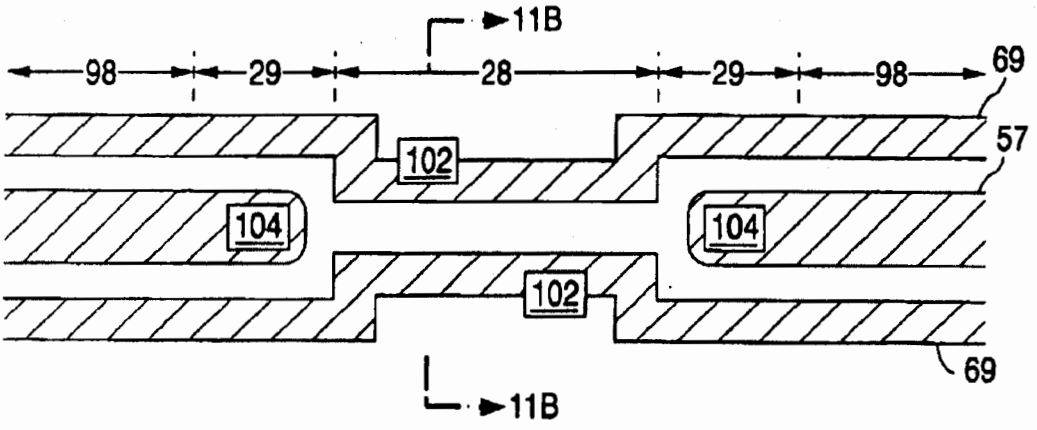

FIG. 11C

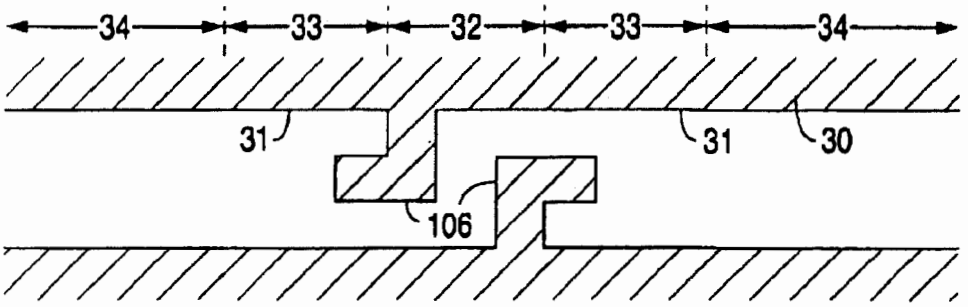

FIG. 12A

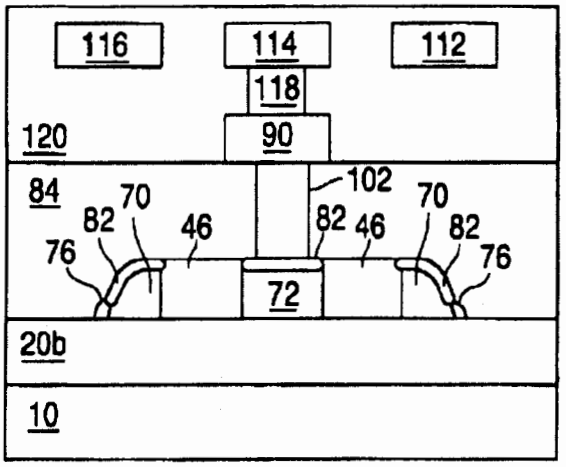

FIG. 12B

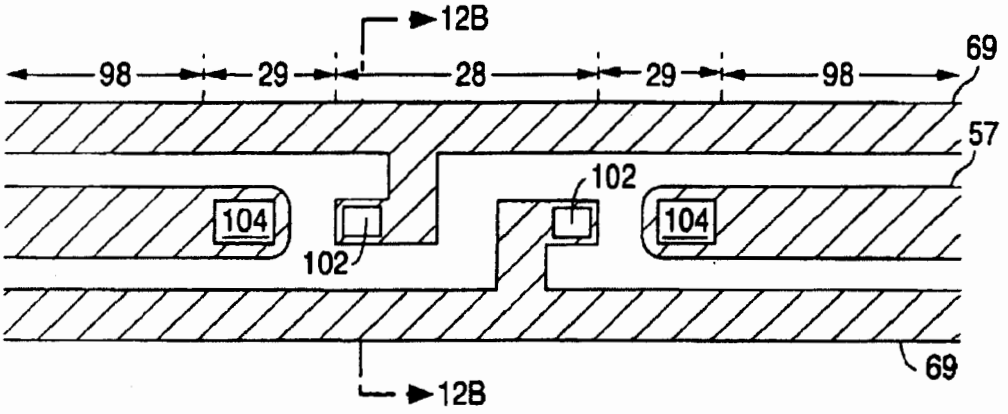

FIG. 12C

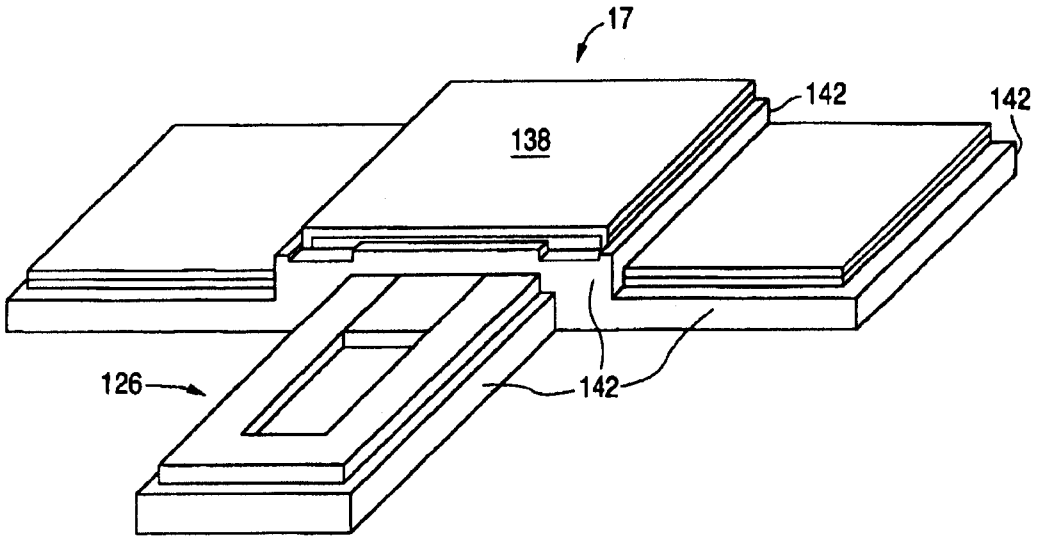

FIG. 13

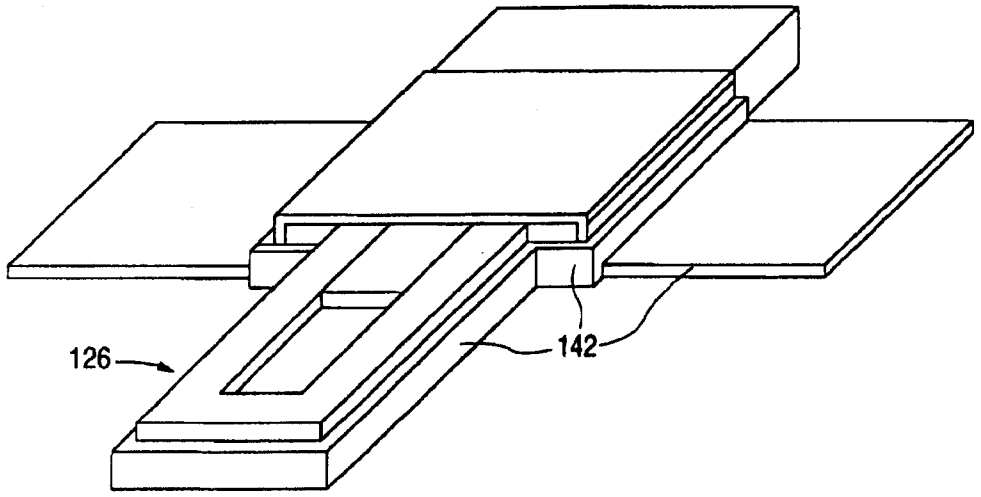

FIG. 16

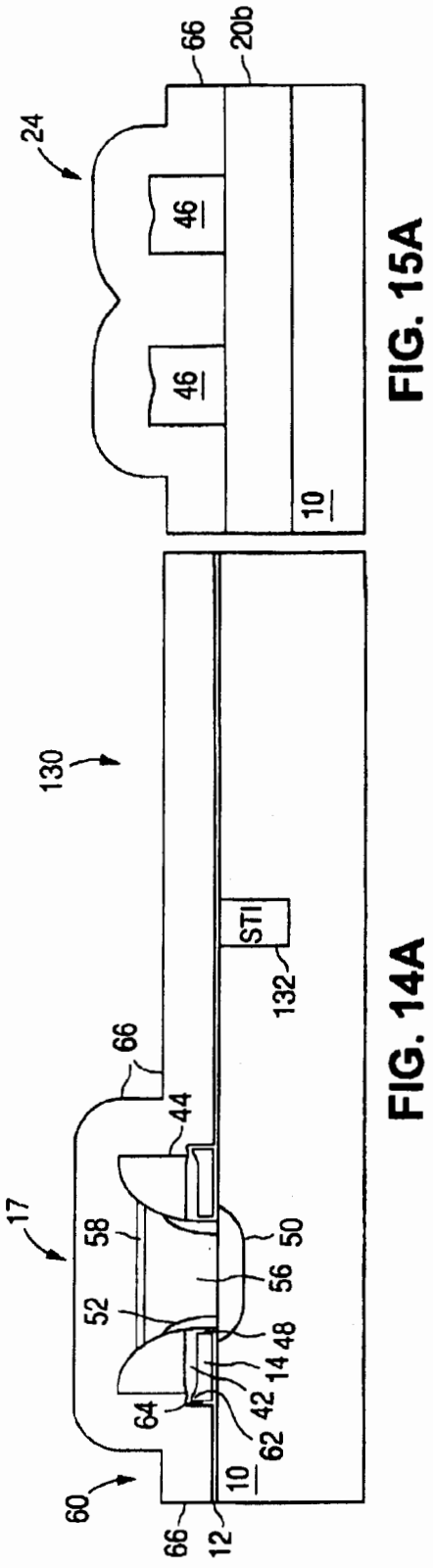

FIG. 15A

FIG. 14A

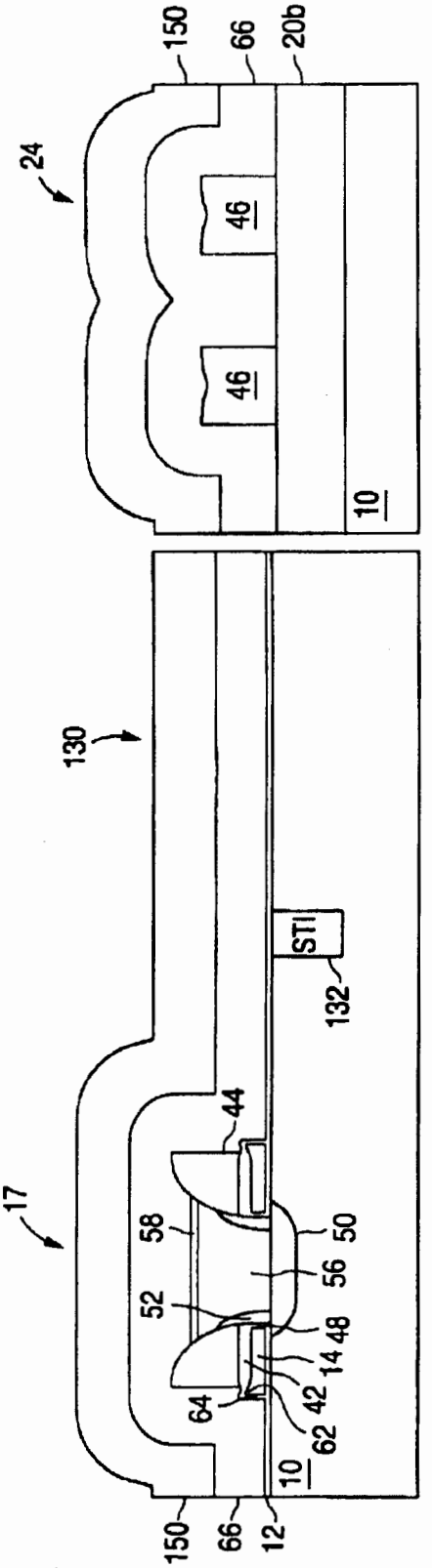

FIG. 15B

FIG. 14B

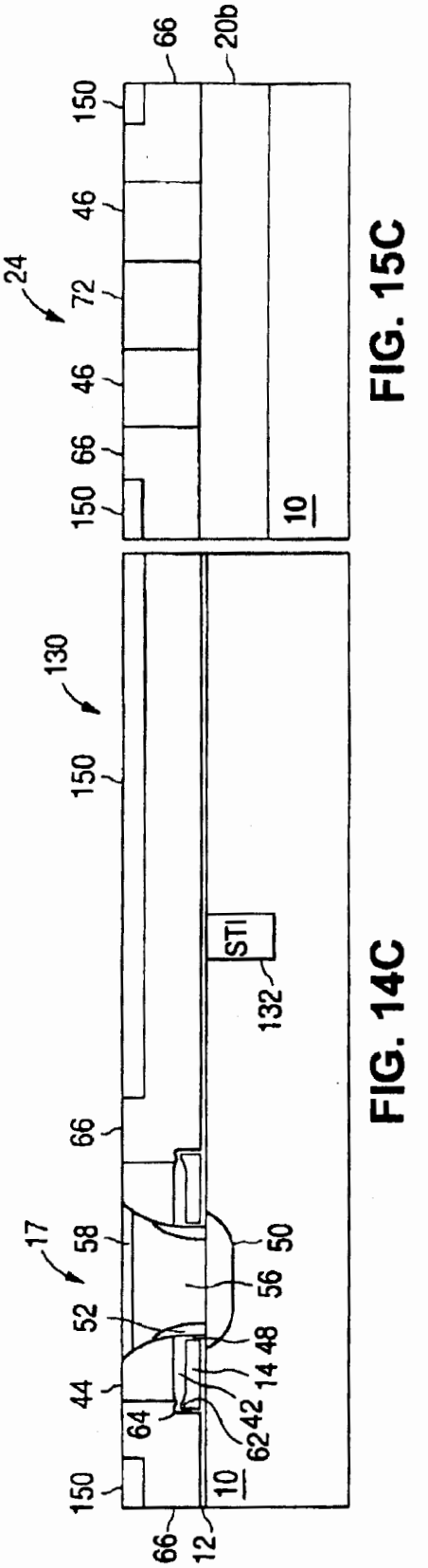

FIG. 14C

FIG. 15C

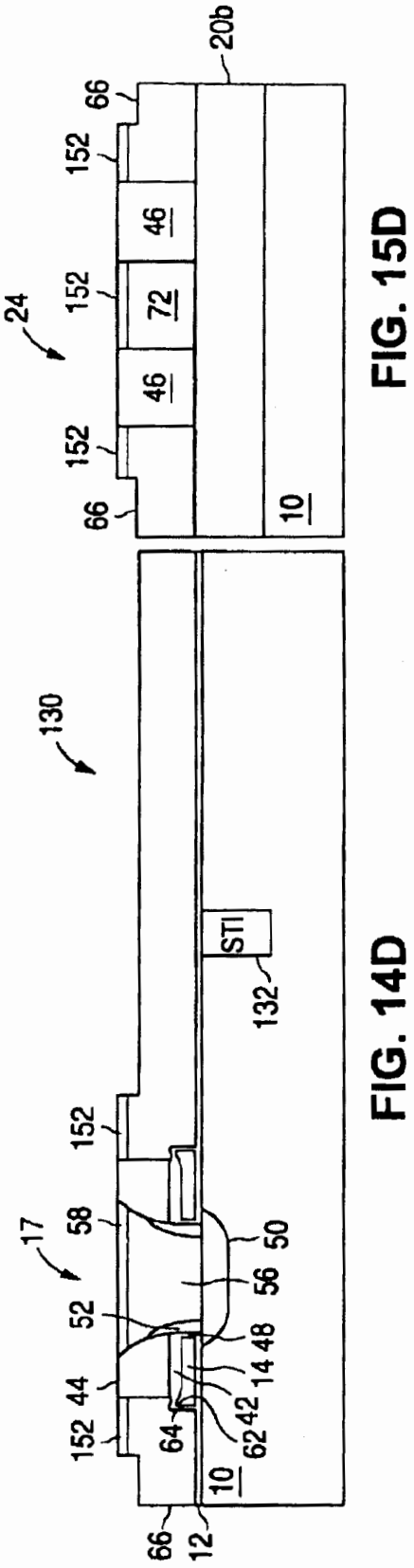

FIG. 14D

FIG. 15D

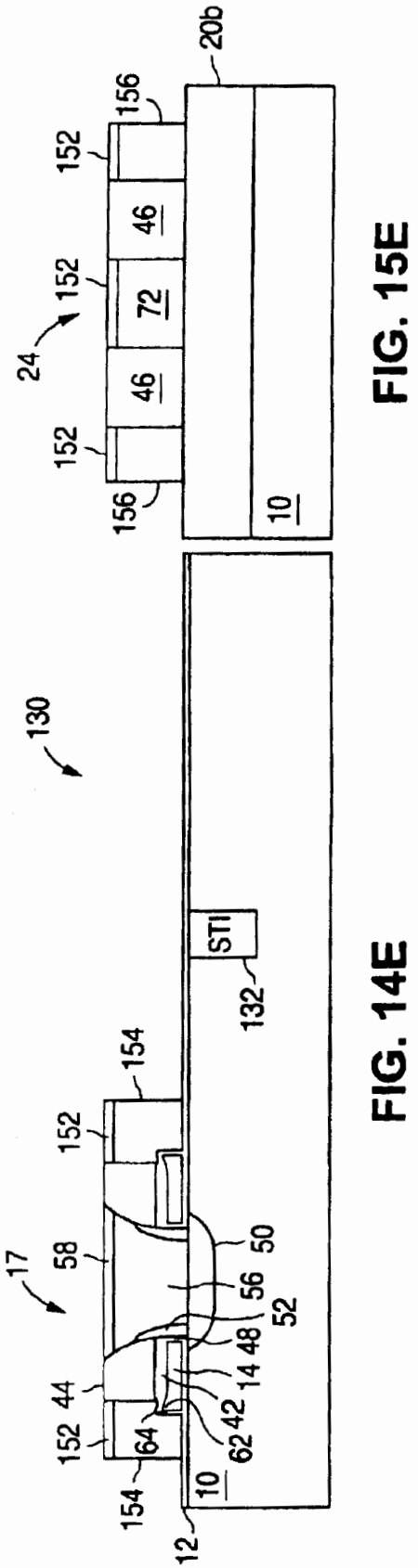

FIG. 14E

FIG. 15E

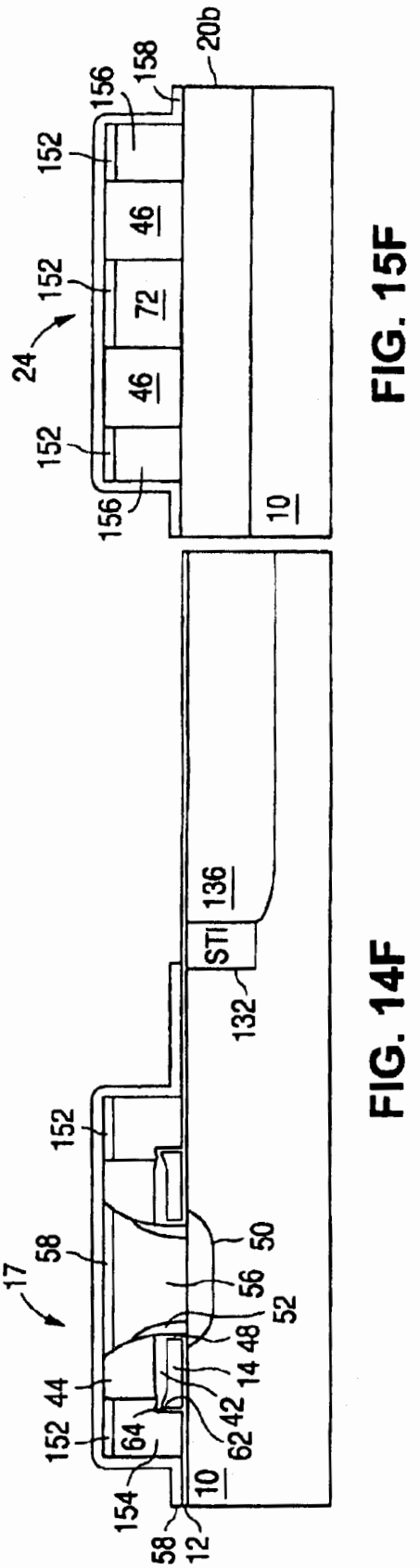

FIG. 14F

FIG. 15F

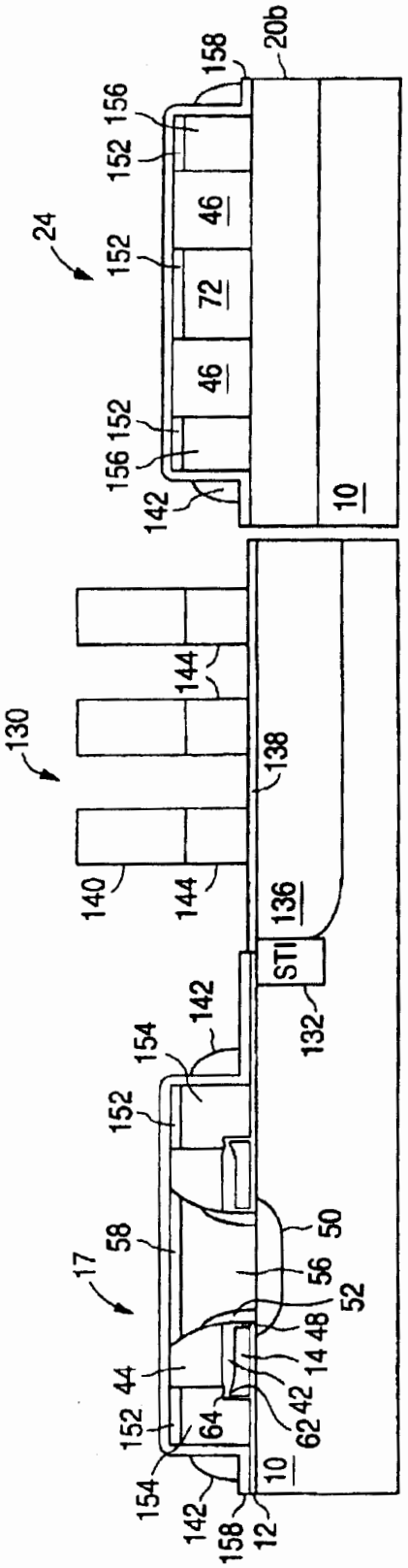

FIG. 14G

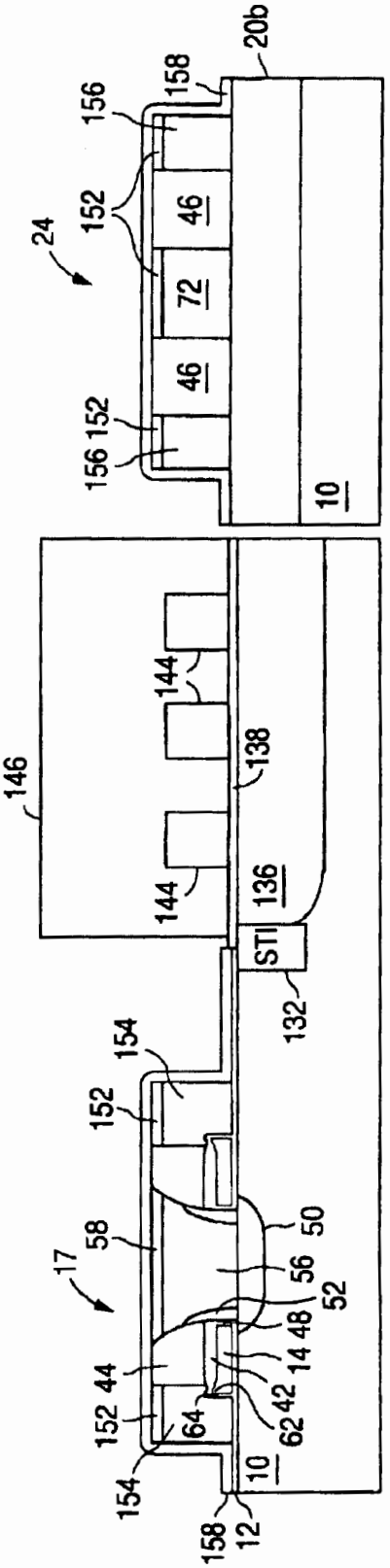

FIG. 14H

FIG. 15G

FIG. 15H

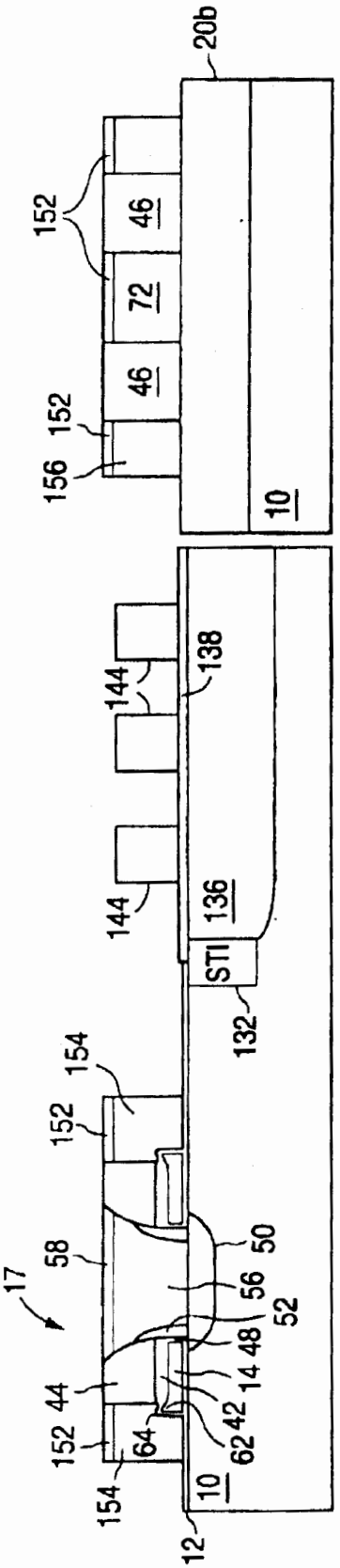

FIG. 15I

FIG. 14I

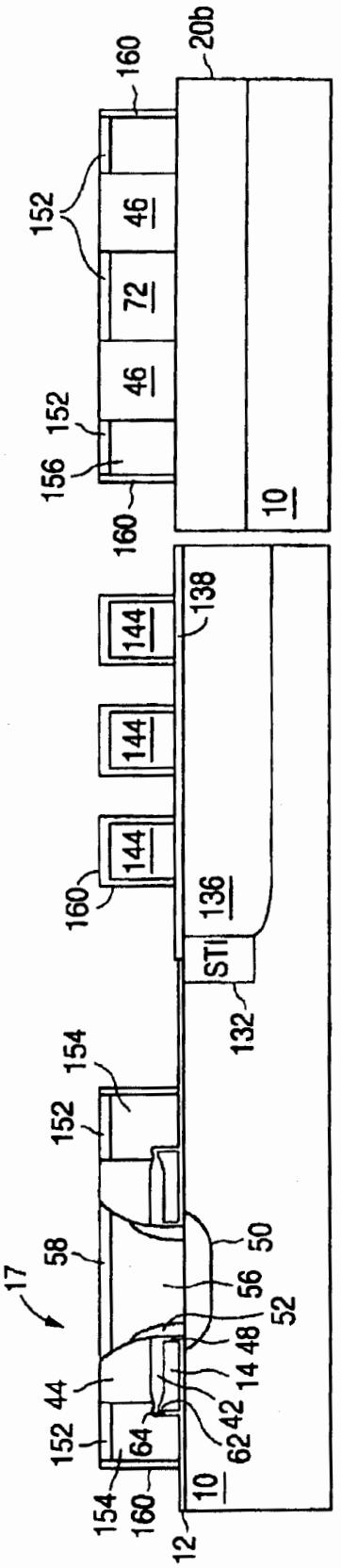

FIG. 15J

FIG. 14J

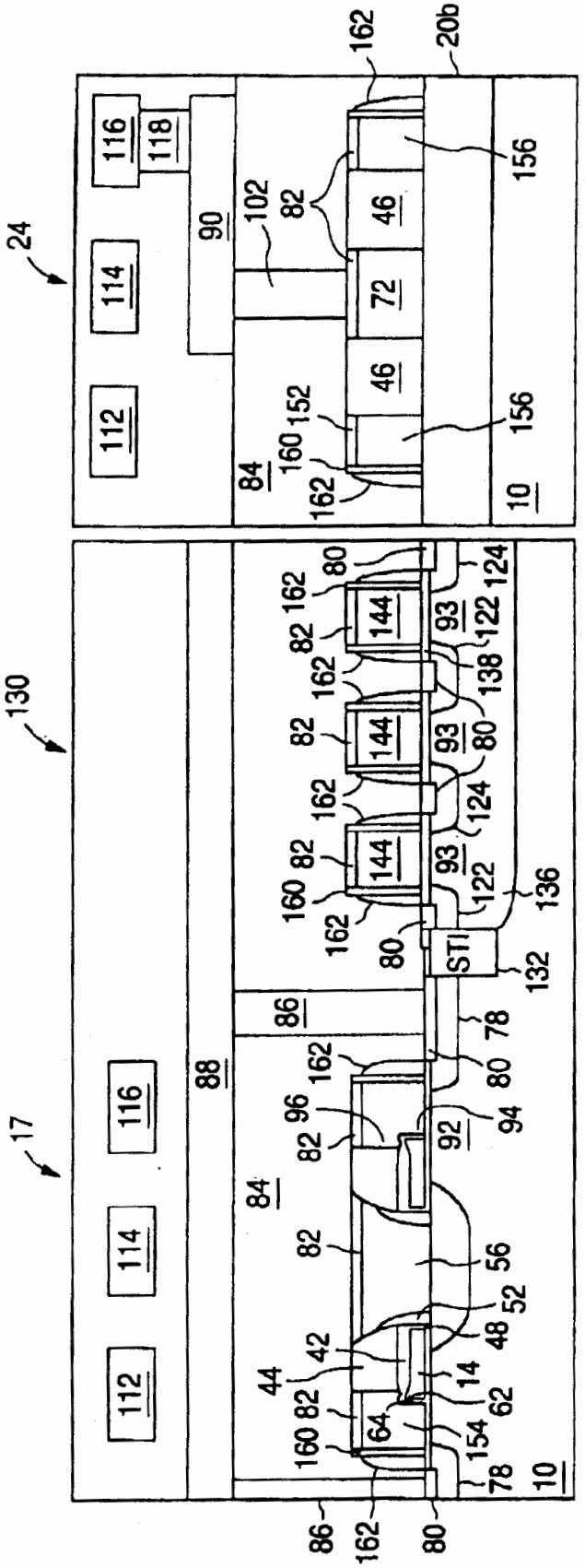

FIG. 14K

FIG. 15K

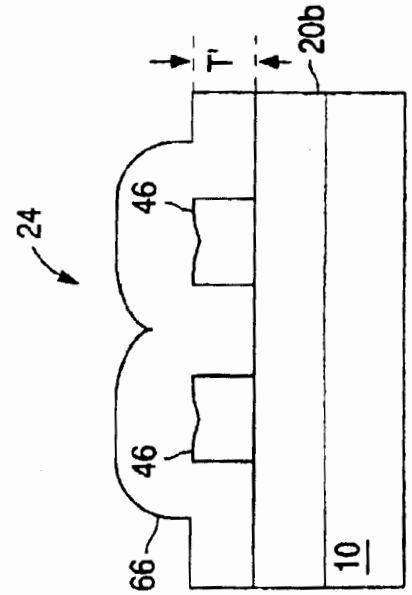

FIG. 18A

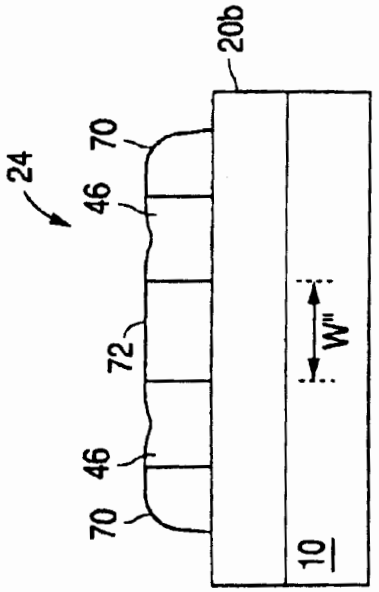

FIG. 18B

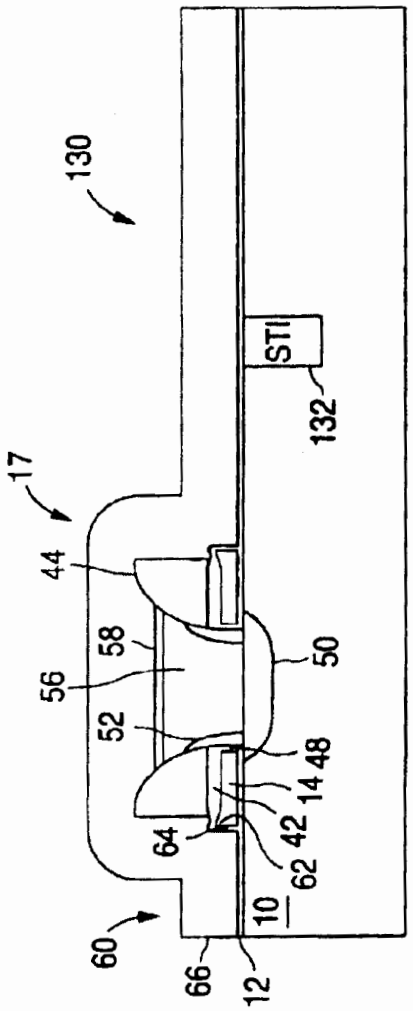

FIG. 17A

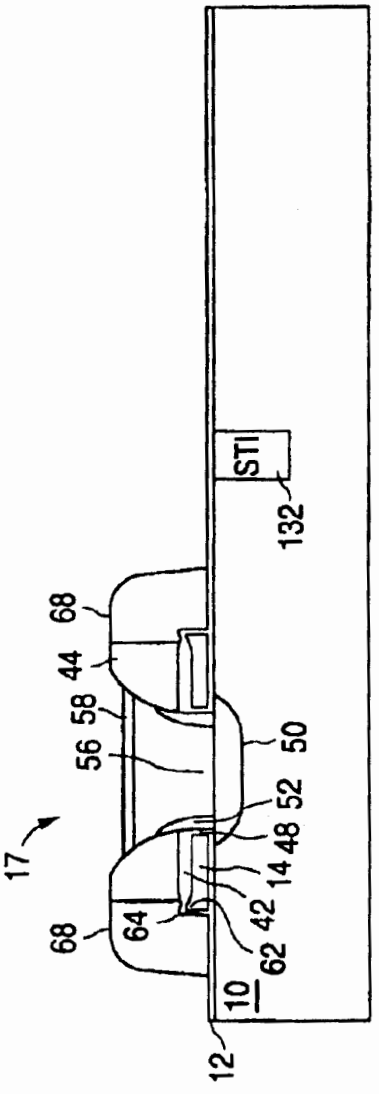

FIG. 17B

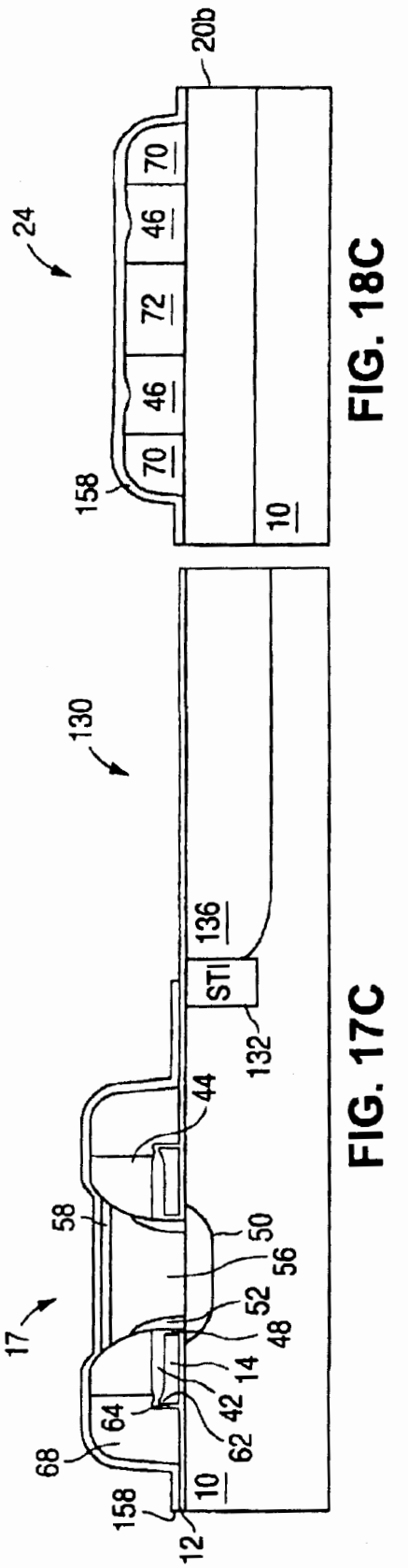

FIG. 17C

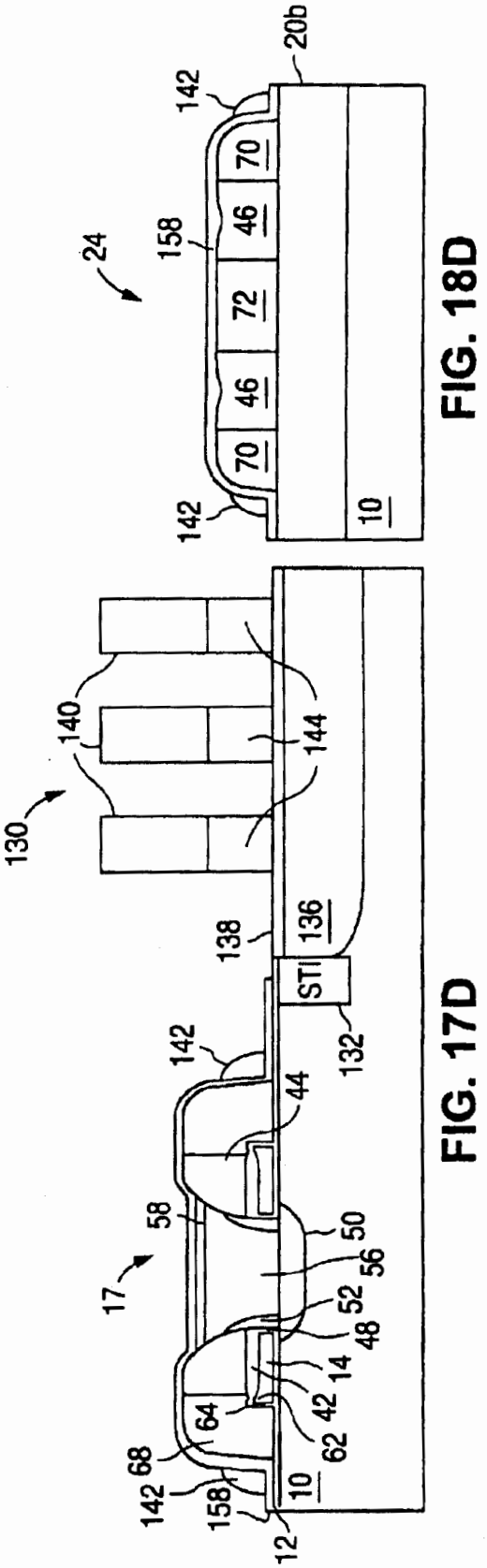

FIG. 17D

FIG. 18C

FIG. 18D

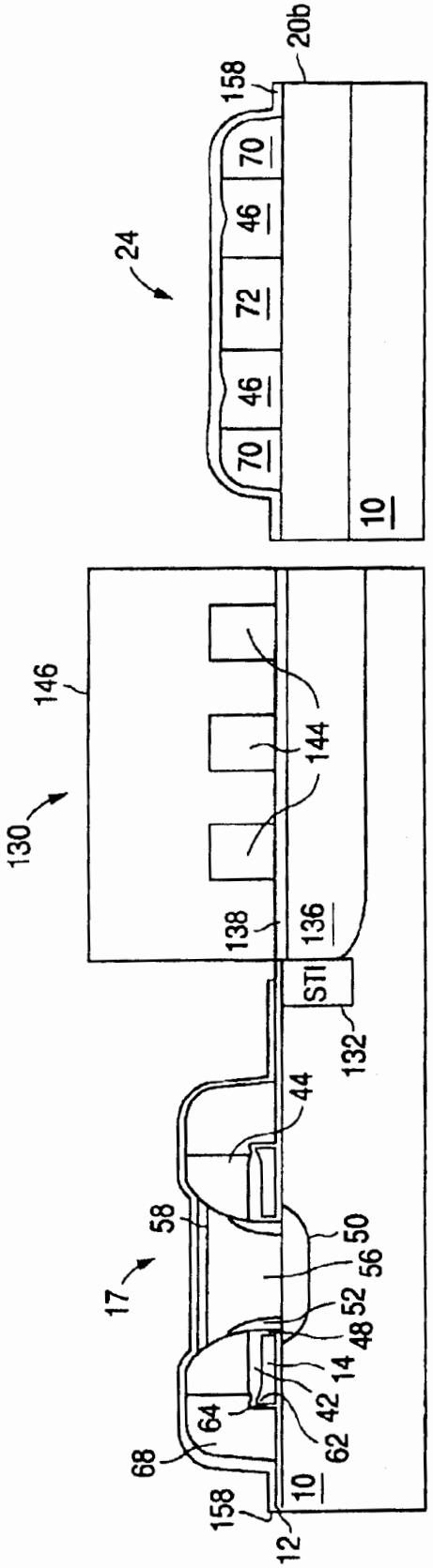

FIG. 18E

FIG. 17E

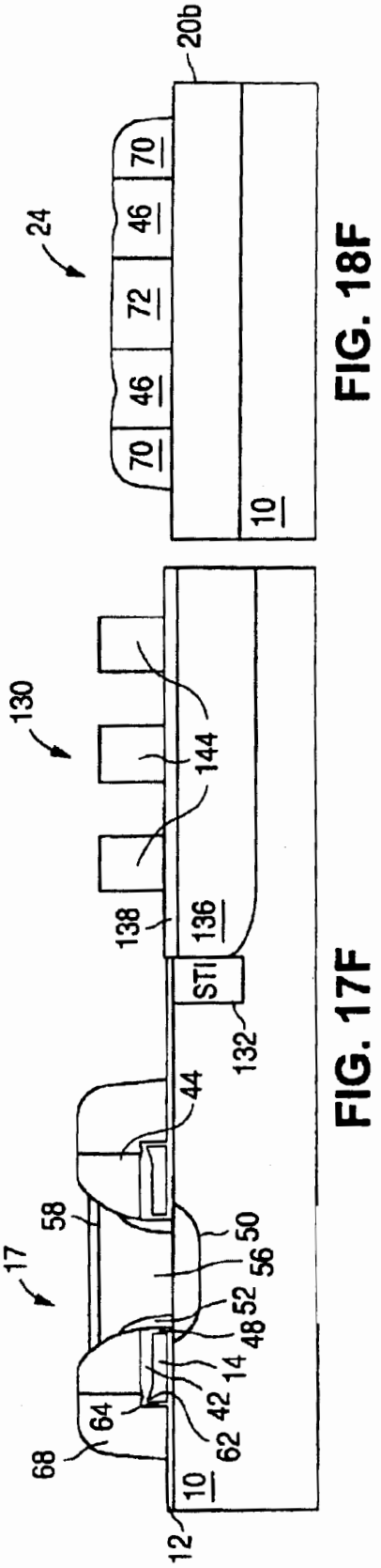

FIG. 18F

FIG. 17F

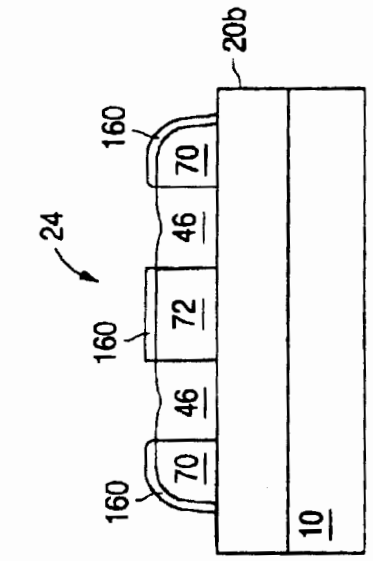

FIG. 18G

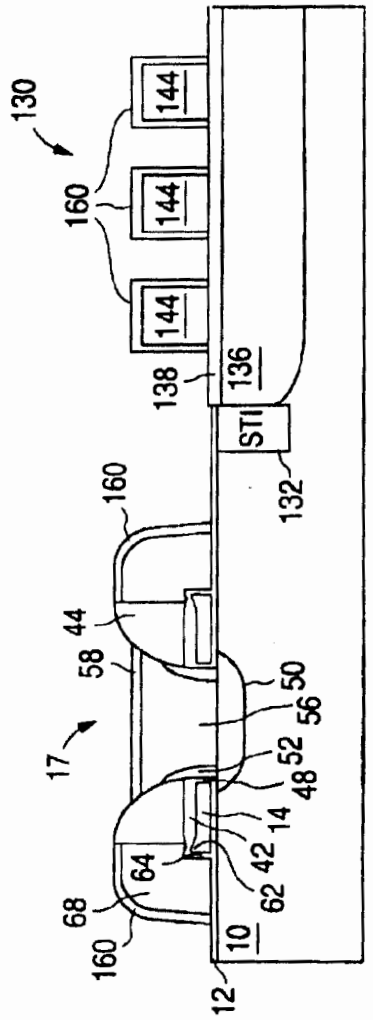

FIG. 17G

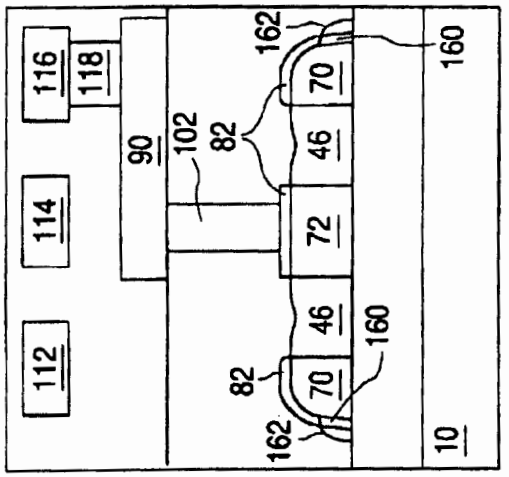

FIG. 18H

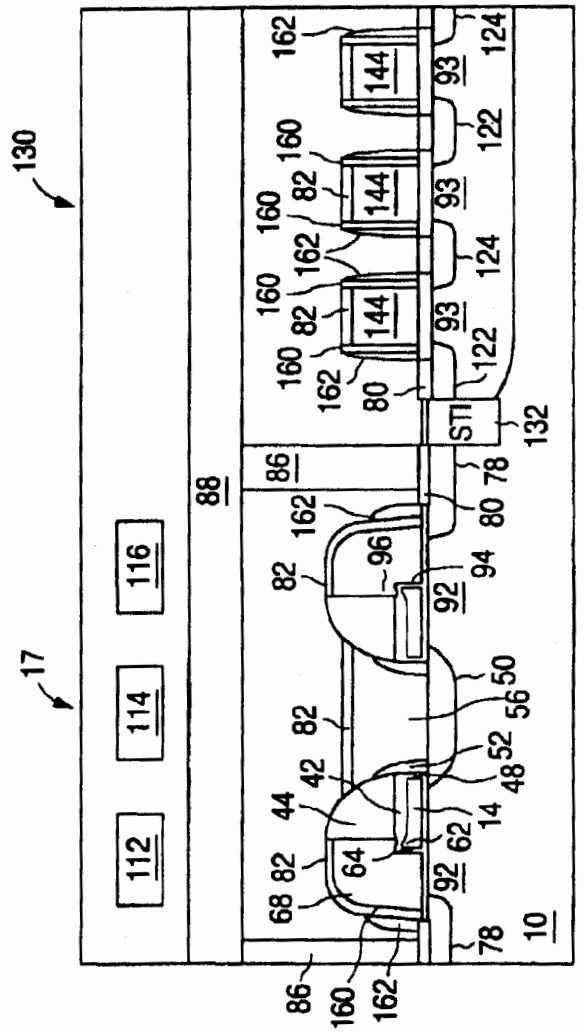

FIG. 17H

METHOD OF FORMING A SEMICONDUCTOR ARRAY OF FLOATING GATE MEMORY CELLS AND STRAP REGIONS, AND A MEMORY ARRAY AND STRAP REGIONS MADE THEREBY

This application claims the benefit of U.S. Provisional Application No. 60/323,445, filed Sep. 18, 2001, and entitled *A Method Integrating A Self-Aligned Flash E2 Prom Cell Into A CMOS Baseline Process.*

TECHNICAL FIELD

The present invention relates to a method of forming strap regions to make electrical contacts with memory cells in an array of semiconductor non-volatile memory cells, and more particularly, in the preferred embodiment, to an array of floating gate memory cells of the split gate type. The present invention also relates to a method of forming a logic or peripheral region on the same semiconductor substrate adjacent the memory cell array, where the structure has a simplified topography, box shaped word poly's, and logic polysilicon elements formed separately from those of the memory cells.

BACKGROUND OF THE INVENTION

Non-volatile semiconductor memory cells using a floating gate to store charges thereon and memory arrays of such non-volatile memory cells formed in a semiconductor substrate are well known in the art. Typically, such floating gate memory cells have been of the split gate type, or stacked gate type, or a combination thereof.

One of the problems facing the manufacturability of semiconductor floating gate memory cell arrays has been the alignment of the various components such as source, drain, control gate, and floating gate. As the design rule of integration of semiconductor processing decreases, reducing the smallest lithographic feature, the need for precise alignment becomes more critical. Alignment of various parts also determines the yield of the manufacturing of the semiconductor products.

Self-alignment is well known in the art. Self-alignment refers to the act of processing one or more steps involving one or more materials such that the features are automatically aligned with respect to one another in that step processing. Accordingly, self alignment minimizes the number of masking steps necessary to form memory cell structures, and enhances the ability to scale such structures down to smaller dimensions.

In the manufacture of memory cell arrays, it is also known to form cell elements that extend across the entire array of memory cells. For example, with an array having interlaced columns of isolation and active regions, with a plurality of memory cells in each active region, memory cell elements such as control gates, source regions, drain regions etc. can be formed to continuously extend across an entire row or column of memory cells. In order to ensure an equalized voltage on such elements for all the memory cells in the target row/column, strap regions have been used to provide multiple electrical connections along the length of continuously formed memory cell elements, so that uniform voltages are applied to all the memory cells in the affected row/column.

FIG. **1** illustrates a known strap region design. Strap region **1** is formed along side a memory cell array **2**. The memory cell array **2** includes columns of active regions **3** interlaced with columns of isolation regions **4**. Rows of

memory cell pairs **5** are formed with word lines **6** and source lines **7** extending along the memory cell rows, with each pair of memory cells having two word lines **6** and sharing a single source line **7**. (Those of skill in the art will recognize that the term source and drain may be interchanged. Further, the word line is connected to the control gate of the floating gate memory cell. Thus, the term control gate or control gate line may also be used interchangeably with the term word line). Typically, the word line and the source lines are made of polysilicon or polysilicide or salicide material. Thus, pure metal lines are used to strap these lines. Strap cells **8** are formed on the control gates **6** and source lines **7** as they traverse the strap region **1**. Electrical contacts **9***a* and **9***b* are then formed onto the control gate (word) lines **6** and source lines **7** respectively by metal lines (not shown) traversing in the word line direction positioned above the array shown in FIG. **1** and electrically insulated therefrom for supplying the desired voltages to the various rows of control gates **6** and source lines **7**.

Ideally, for larger memory arrays, a plurality of strap regions are interlaced within the memory cell array (e.g. one strap region for every 128 cells in the word line direction). Preferably, the strap regions are formed simultaneously with the process steps used to make the memory cell array.

As device geometries get smaller, it is increasingly difficult to reliably form electrical connections to the strap regions **8**. The word lines **6** are very close to the source lines **7**, and get even closer with smaller device geometries. As the distance between the control gate lines **6** and source line **7** shrinks, it becomes more difficult to form contacts **9***a* and **9***b* properly. For example, just a small shift of one of the control gate line **6** contacts toward an adjacent source line **7** would result in the contact being formed over both a word line **6** and a source line **7**, thus shorting the two together. Further, there is simply no room to enlarge and separate the strap cells to increase the tolerance of the contact formation steps.

One or more logic or peripheral regions are formed adjacent to the memory cell array on the same silicon substrate. Logic devices (i.e. MOS FET's, etc.) are formed in these regions to operate the memory cell array or perform logic functions related to the memory cell array. In order to form such logic devices along side the memory cell array, the topography of the resulting structure can be complex, resulting in the formation of unwanted layers and spacers that are difficult to remove once the structure formation is complete. Further, certain elements of the logic devices and memory cells are often formed with the same processing steps, thus coupling the formation of these elements together. This can make it difficult to optimize elements of the logic devices without adversely affecting elements of the memory cells, and vice versa.

Thus, there is a need for a strap cell design, and a manufacturing method thereof, that minimizes the risk of shorting source lines **7** and word lines **6** together during the formation of the strap cells, and/or during the formation of electrical contacts connected thereto. There is also a need to form such strap cells using the same processing steps that are used to form the memory cells in the active regions. Further, there is a need to form a logic/peripheral region adjacent the memory cell array where the structure has a simplified topography, box shaped word line poly's, and logic poly's formed separately from those in the memory cells.

SUMMARY OF THE INVENTION

The present invention provides a memory cell array with a strap region that minimizes the risk of shorting the source

and word lines together, maximizes the spacing of contacts in the strap region to enable further scaling of device geometries, and provides for logic devices formed in a decoupled manner and in a manner such that the structure has a simplified topography.

The method of the present invention includes the steps of forming a plurality of memory cells in a memory portion of a semiconductor substrate, forming a layer of protective material over control gates of the memory cells, forming a plurality of logic devices that includes forming residual conductive material on the layer of protective material, and removing the residual conductive material. The formation of each of the memory cells includes the steps of forming a floating gate of conductive material disposed over and insulated from the memory portion of the substrate, and forming a control gate of conductive material disposed over and insulated from the memory portion of the substrate. The layer of protective material is formed over the control gates. The plurality of logic devices are formed in a peripheral region of the semiconductor substrate after the formation of the protective material layer. The formation of each of the logic devices includes the step of forming a block of conductive material disposed over and insulated from the peripheral region of the substrate. The formation of the blocks of conductive material includes the formation of the residual conductive material on the layer of protective material. The residual conductive material is removed without removing the conductive material of the control gates.

Other objects and features of the present invention will become apparent by a review of the specification, claims and appended figures.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a top view of an array of non volatile memory cells, and a conventional strap region formed adjacent thereto.

FIG. **2**A is a top view of a semiconductor substrate used in the first step of the method of present invention to form isolation regions.

FIG. **2**B is a cross sectional view of the structure taken along the line **1**—**1** showing the initial processing steps of the present invention.

FIG. **2**C is a top view of the structure showing the next step in the processing of the structure of FIG. **2**B, in which isolation regions are formed.

FIG. **2**D is a cross sectional view of the structure in FIG. **2**C taken along the line **1**—**1** showing the trenches to be formed as isolation stripes in the structure.

FIG. **2**E is a cross sectional view of the structure in FIG. **2**C taken along the line **1**—**1** showing the two types of isolation regions that can be formed in the semiconductor substrate: LOCOS or shallow trench.

FIGS. **3**A–**3**S are cross sectional views taken along the line **2**—**2** of FIG. **2**C showing in sequence the next step(s) in the processing of the structure shown in FIG. **2**C, in the formation of a non volatile memory array of floating memory cells of the split gate type.

FIGS. **4**A–**4**S are cross sectional views of the strap regions showing in sequence the next step(s) in the processing of the strap region structure imaged by the line **4**B—**4**B portion of the mask of FIG. **5**.

FIG. **5** is a top view of a portion of the mask used to form the first trenches in the active regions and the 'H' shaped strap cells in the strap regions.

FIG. **6**A is a cross sectional view of the completed strap region structure imaged by the line **6**A—**6**A portion of the mask of FIG. **5**.

FIG. **6**B is a cross sectional view of the completed strap region structure imaged by the line **6**B—**6**B portion of the mask of FIG. **5**.

FIG. **6**C is a cross sectional view of the completed strap region structure along the line **6**C—**6**C of FIG. **7**.

FIG. **7** is a top plan view of the strap cells and adjacent memory cell arrays of the present invention.

FIG. **8** is a top plan view of a WL strap cell and SL strap cell structure of the strap region of the present invention.

FIG. **9**A is a top view of a first alternate embodiment of the mask, which is used to form the first trenches in the active regions and the 'S' shaped strap cell in the strap regions.

FIG. **9**B is a cross sectional view of the 'S' shaped strap region structure along line **9**B—**9**B in FIG. **9**C.

FIG. **9**C is a top view of the 'S' shaped strap cell structure.

FIG. **10**A is a top view of a second alternate embodiment of the mask, which is used to form the first trenches in the active regions and the '$' shaped strap cell in the strap regions.

FIGS. **10**B and **10**C are cross sectional views of the '$' shaped strap region structure, along lines **10**B—**10**B and **10**C—**10**C respectively in FIG. **10**D.

FIG. **10**D is a top view of the '$' shaped strap cell structure.

FIG. **11**A is a top view of a third alternate embodiment of the mask, which is used to form the first trenches in the active regions and the 'I' shaped strap cell in the strap regions.

FIG. **11**B is a cross sectional view of the 'I' shaped strap region structure, along line **11**B—**11**B in FIG. **11**C.

FIG. **11**C is a top view of the 'I' shaped strap cell structure.

FIG. **12**A is a top view of a fourth alternate embodiment of the mask, which is used to form the first trenches in the active regions and the 'S' shaped strap cell in the strap regions.

FIG. **12**B is a cross sectional view of the 'S' shaped strap region structure, along line **12**B—**12**B in FIG. **12**C.

FIG. **12**C is a top view of the 'S' shaped strap cell structure.

FIG. **13** is a perspective view of the active region structure of FIG. **3**P.

FIGS. **14**A–**14**K are cross sectional views taken along the line **2**—**2** of FIG. **2**C showing in sequence the step(s) in the first alternate embodiment of the processing of the structure shown in FIG. **3**L, in the formation of a non volatile memory array of floating memory cells of the split gate type.

FIGS. **15**A–**15**K are cross sectional views of the strap regions showing in sequence the step(s) in the first alternate embodiment of the processing of the strap region structure of FIG. **4**L.

FIG. **16** is a perspective view of the active region structure of FIG. **14**G.

FIGS. **17**A–**17**H are cross sectional views taken along the line **2**—**2** of FIG. **2**C showing in sequence the step(s) in the second alternate embodiment of the processing of the structure shown in FIG. **3**L, in the formation of a non volatile memory array of floating memory cells of the split gate type.

FIGS. **18**A–**18**H are cross sectional views of the strap regions showing in sequence the step(s) in the second alternate embodiment of the processing of the strap region structure of FIG. **4**L.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention is an array of non-volatile memory cells having a strap cell design, and method of making such strap cells, with enhanced contact formation. The strap cells are formed using the same processing steps that are used to form the array of memory cells. The strap cell regions containing the strap cells are interlaced among an array of non-volatile memory cells having word lines and source lines that extend across rows of memory cells. Co-pending patent application Ser. No. 09/917,023, filed on Jul. 26, 2001, which is commonly assigned to the assignee of the present invention, and whose disclosure is hereby incorporated by reference herein, discloses a self aligned method of forming a split gate non-volatile memory cell array. In the preferred embodiment, the strap cell regions of the present invention will be disclosed in the context of forming such a split gate non-volatile memory cell array, although it should be apparent that the present invention can also be practiced with other types of array of memory cells, in which the array is traversed by a row of source (or drain) line and parallel thereto a row of word line. The present invention also includes a logic devices formed in a logic/peripheral region adjacent to the memory cell array having a simplified topography and formed in a decoupled manner so that the poly elements of the logic devices and the memory cells can be separately optimized.

Isolation Region Formation

Referring to FIG. **2**A there is shown a top plan view of a semiconductor substrate **10** (or a semiconductor well), which is preferably of P type and is well known in the art. A first layer of insulation material **12**, such as silicon dioxide (oxide), is deposited thereon as shown in FIG. **2**B. The first insulation layer **12** is formed on the substrate **10** by well known techniques such as oxidation or deposition (e.g. chemical vapor deposition or CVD), forming a layer of oxide preferably 80 Å thick. A first layer of polysilicon **14** (hereinafter "poly") is deposited on top of the first layer of insulation material **12** (e.g. 700 to 800 Å thick). The deposition and formation of the first polysilicon layer **14** on the first insulation layer **12** can be made by a well known process such as Low Pressure CVD or LPCVD. A silicon nitride layer **18** (hereinafter "nitride") is deposited over the polysilicon layer **14**, preferably by CVD (e.g. 1000 Å thick). This nitride layer **18** is used to define the active regions during isolation formation. Of course, all of the forgoing described parameters and the parameters described hereinafter, depend upon the design rules and the process technology generation. What is described herein is for the 0.18 micron process. However, it will be understood by those skilled in the art that the present invention is not limited to any specific process technology generation, nor to any specific value in any of the process parameters described hereinafter.

Once the first insulation layer **12**, the first polysilicon layer **14**, and the silicon nitride **18** have been formed, suitable photo-resistant material **19** is applied on the silicon nitride layer **18** and a masking step is performed to selectively remove the photo-resistant material from certain regions (stripes **16**). Where the photo-resist material **19** is removed, the silicon nitride **18**, the polysilicon **14** and the underlying insulation material **12** are etched away in stripes **16** formed in the Y or column direction, as shown in FIG. **2**C, using standard etching techniques (i.e. anisotropic etch processes). The distance W between adjacent stripes **16** can be as small as the smallest lithographic feature of the process

used. Where the photo resist **19** is not removed, the silicon nitride **18**, the first polysilicon region **14** and the underlying insulation region **12** are maintained. The resulting structure is illustrated in FIG. **2**D, with active regions **17** interlaced with isolation regions **16**. As will be described, there are two embodiments in the formation of the isolation regions: LOCOS and STI. In the STI embodiment, the etching continues into the substrate **10** to a predetermined depth.

The structure is further processed to remove the remaining photo resist **19**. Then, an isolation material **20***a* or **20***b*, such as silicon dioxide, is formed in the regions or "grooves" **16**. The nitride layer **18** is then selectively removed to form the structure shown in FIG. **2**E. The isolation can be formed via the well known LOCOS process resulting in the local field oxide **20***a* (e.g. by oxidizing the exposed substrate), or it can be formed via a shallow trench process (STI) resulting in silicon-dioxide being formed in the region **20***b* (e.g. by depositing an oxide layer, followed by a Chemical-Mechanical-Polishing or CMP etch). It should be noted that during the LOCOS formation, a spacer may be necessary to protect the side walls of poly layer **14** during the formation of the local field oxide.

The remaining first polysilicon layer **14** and the underlying first insulation material **12** form the active regions. Thus, at this point, the substrate **10** has alternating stripes of active regions and isolation regions with the isolation regions being formed of either LOCOS insulation material **20***a* or shallow trench insulation material **20***b*. Although FIG. **2**E shows the formation of both a LOCOS region **20***a* and a shallow trench region **20***b*, only one of the LOCOS process (**20***a*) or the shallow trench process (**20***b*) will be used. In the preferred embodiment, the shallow trench **20***b* will be formed. Shallow trench **20***b* is preferable because it can be more precisely formed at smaller design rules.

The structure in FIG. **2**E represents a self aligned structure, which is more compact than a structure formed by a non self-aligned method. A non self-aligned method of forming the structure shown in FIG. **2**E, which is well known and is conventional, is as follows. Regions of isolation **20** are first formed in the substrate **10**. This can be done by depositing a layer of silicon nitride on the substrate **10**, depositing photo-resist, patterning the silicon nitride using a first masking step to expose selective portions of the substrate **10**, and then oxidizing the exposed substrate **10** using either the LOCOS process or the STI process where silicon trench formation and trench fill are involved. Thereafter, the silicon nitride is removed, and a first layer of silicon dioxide **12** (to form the gate oxide) is deposited over the substrate **10**. A first layer of polysilicon **14** is deposited over the gate oxide **12**. The first layer of polysilicon **14** is then patterned using a second masking step and selective portions removed. Thus, the polysilicon **14** is not self aligned with the regions of isolation **20**, and a second masking step is required. Further, the additional masking step requires that the dimensions of the polysilicon **14** have an alignment tolerance with respect to the regions of isolation **20**. It should be noted that the non self-aligned method does not utilize nitride layer **18**.

In the above processing steps, one or more isolation regions are designated as strap regions **24** (see description of FIG. **4**A below), in which strap cells for the word lines and source lines will be formed. Again, as used herein, the term source line is meant to include drain line as well. The width of the strap regions **24** is preferably wider than the width of the isolation regions **16** to accommodate the formation of the strap cells therein. Thus, the resulting structure includes sets of interlaced columns of active and isolation regions, with columns of strap regions **24** interlaced between the sets of

active/isolation regions. In the preferred embodiment, a strap region column is formed between every set of 128 or 256 active and isolation regions **17/16**.

Memory Array Formation

With the structure shown in FIG. **2**E made using either the self aligned method or the non self-aligned method, the structure is further processed as follows. FIGS. **3**A to **3**S show the cross section of the active region structure **17** from a view orthogonal to that of FIGS. **2**B and **2**E, and FIGS. **4**A to **4**S show the cross section of the strap region structure **24** from the same orthogonal view, as the next steps in the process of the present invention are performed concurrently on both regions. It should be appreciated that while only a single active region **17** and single **24** strap region are shown, the processing steps illustrated below form an array of such regions.

An insulation layer **22** is first formed on the structure. Specifically, a nitride layer **22** is deposited across the entire surface of the structure (e.g. 3000 Å thick). The resulting active region structure is shown in FIG. **3**A, and the resulting strap region structure is shown in FIG. **4**A.

A masking operation is performed on both the active/isolation regions **17/16** and the strap region **24**, by first applying photo-resist **23** on top of the nitride layer **22**. A masking step is applied to the structure using a mask **30**, as illustrated in FIG. **5**. Mask **30** is formed of an opaque masking material (such as metal) that contains a patterned aperture **31** for defining masking regions on the structure from which material is to be removed. Mask **30** includes a first mask region **32** (for defining the word line (WL) strap cells), a second mask region **33** (for defining the source line (SL) strap cells), and a third mask region **34** (for forming the memory cell array). The mask **30** shown in FIG. **5** is used to define a single strap region row and single row of memory cells. Thus, a mask having an array of geometries **30** is used to define the memory cell array including the strap regions of the present invention.

The mask regions **34** include single linear apertures for defining parallel stripe masking regions over the active and isolation regions **17/16**, which extend in the X or the row direction. The distance between adjacent stripes can be a size determined by the needs of the device to be fabricated. After mask regions **34** are imaged onto the active regions **17** (shown in FIG. **3**A), the photo resist **23** in the exposed masking regions is removed (i.e. stripes in the row direction), leaving rows of the nitride layer **26** exposed. The exposed nitride layer portions are removed using a nitride anisotropic etch process until the poly layer **14** is observed, which acts as an etch stop. The portions of layers **12**, **14** and **22** still underneath the remaining photo resist **23** are unaffected by this etch process. It will become evident from the following description that the process of the present invention creates columns of multiple pairs of mirror memory cells. For each such pair of memory cells, this nitride etch process results in the formation of a single first trench **26** that extends down to polysilicon layer **14**, as shown in FIG. **3**B.

The mask regions **32** each include a single transparent linear aperture into which a pair of opaque L shaped members **35** protrude. Members **35** extend out from opposing sides of aperture **31**, and bend toward each other, to form an 'H' shaped aperture (the shape in the form of the letter 'H' can be seen by rotating FIG. **5** by 90 degrees). Mask regions **32** are used to define WL strap cells in the strap regions **24** that are each aligned to one of the rows of memory cells in the array. The mask regions **32** are imaged onto the strap regions **24**, where an 'H' shaped trench pattern is formed in each row of the strap regions **24** by the nitride anisotropic etch step. FIG. **4**B illustrates the cross section view of the strap regions **24** after the nitride etch step, that are imaged by the line **4**B—**4**B portion of the 'H' shaped mask pattern of FIG. **5**. The two parallel portions of the 'H' shaped pattern result in the formation of a pair of trenches **40** in the strap regions **24**, as shown in FIG. **4**B.

The mask regions **33** each include a single linear aperture for forming the SL strap cells in the strap regions **24**. Each SL strap cell is aligned to one of the rows of memory cells in the array. The mask regions **33** are each imaged down onto the structure between one of the 'H' shaped trench patterns and one of the rows of memory cells, as later described and illustrated.

The residual photo-resist **23** is removed from the structure, which is followed by an oxidation process. For the active region **17**, this oxidation process oxidizes the exposed portions of poly layer **14** inside of trenches **26** to form a lens shaped oxide layer **42** over poly layer **14** (see FIG. **3**C). While not shown, an optional poly etch process can be performed before the formation of layer **42**. This optional customized anisotropic poly etch process etches away a portion of the top surface of poly layer **14**, but leaves a taper shape in that top surface in the area next to the remaining nitride layer **22**. Oxide spacers **44** are then formed inside trenches **26**. The formation of spacers is well known in the art, and includes depositing a material over the contour of a structure (as shown in FIG. **3**C), followed by an anisotropic etch process (e.g. RIE), whereby the material is removed from horizontal surfaces of the structure, while the material remains largely intact on vertically oriented surfaces of the structure. To form oxide spacers **44**, a thick layer of oxide is deposited over the structure, followed by an anisotropic oxide etch, which removes the deposited oxide except for spacers **44** inside trenches **26**. This oxide etch step also removes the center portion of oxide layer **42** from each of the trenches **26**. The oxide etch step uses the nitride layer **22** as the etch stop. The resulting structure in the active region **17** is shown in FIG. **3**D.

For the strap region **24**, the oxidation process used to form oxide layer **42** in the active region **17** has no affect. The oxide deposition and etch steps used to form spacers **44** in the active region end up filling trenches **40** in the strap region **24** with oxide to form oxide blocks **46**. Specifically, the oxide deposition completely fills trenches **40** (see FIG. **4**C) and the oxide etch removes the oxide outside of trenches **40** (see FIG. **4**D). Trenches **40** are filled solid with oxide instead of with oxide spacers along their sidewalls so long as trenches **40** have a sufficiently narrow width W'. For example, in many applications, if the width W' of each trench **40** is no greater than approximately twice the thickness T of the deposited oxide, then the trenches **40** will be filled with oxide to form oxide blocks **46**. Therefore, for the preferred embodiment, the width of the trenches in the trench pattern formed by imaging patterned aperture onto the strap region **24** is narrow enough to ensure that the trench pattern is filled with oxide by the oxide deposition/etch steps.

An anisotropic poly etch process is then performed on the structure. For the active region **17**, this etch removes portions of the poly layer **14** that are exposed between the opposing insulation spacers **44** at the bottom of trenches **26**. The oxide layer **12** acts as an etch stop. This poly etch has no effect on the strap region. A thin oxide etch is then performed, which removes the exposed portions of thin oxide layer **12** between spacers **44** at the bottom of trenches **26** to expose substrate **10**. The use of spacers **44** allows the

formation of trenches **26** having a width at the poly layer **14** that is less than the width of the masking step used to initially define the tops of trenches **26**. The resulting active region structure is illustrated in FIG. **3**E. The oxide etch removes a negligible amount of the oxide blocks **46** in strap region **24**, as shown in FIG. **4**E.

An oxidation step is then performed, where in the active region **17**, the sides of polysilicon layer **14** and the substrate surface that are exposed inside trenches **26** are oxidized to form oxide side walls **48** on the sides of poly layer **14** and to reform oxide layer **12** over the substrate **10** exposed inside trenches **26**. Suitable ion implantation is then made across the entire surface of the structure. Where the ions have sufficient energy to penetrate the oxide layer **12** in trenches **26**, they then form a first region (i.e. source region) **50** in the substrate **10**. In all other regions, the ions are absorbed by the existing structure, where they have no effect. Insulation (e.g. oxide) spacers **52** are then formed inside trenches **26** by depositing a layer of oxide, followed by an anisotropic oxide etch, which removes the deposited oxide except for spacers **52**. This oxide etch step also removes the center portion of oxide layer **12** from each of the trenches **26** to re-expose the substrate **10**. The resulting active region structure is shown in FIG. **3**F. The above described oxidation, ion implantation, and oxide deposition/etch steps have no appreciable net affect on the strap region structure **24**, as shown in FIG. **4**F.

A poly deposition step is then performed, leaving a thick layer **54** of polysilicon over the active region **17** and strap region **24**, as shown in FIGS. **3**G and **4**G, respectively. A poly planarization step follows (preferably CMP), which etches the poly layer **54** down to nitride layer **22**, leaving poly blocks **56** in trenches **26** (in the active region **17**). A poly etch-back step follows to recess the top portion of poly blocks **56** below the tops of trenches **26**, to remove any excess polysilicon outside of trenches **26** (and any polysilicon remaining in the strap region **24**). The polysilicon is properly doped either through an in-situ method or by conventional implantation. An oxide layer **58** is then formed by oxidizing the top portions of poly blocks **56**, which has no affect on strap region **24**. The resulting active region structure is shown in FIG. **3**H, and the resulting strap region structure is shown in FIG. **4**H.

A nitride etch is then performed to remove nitride layer **22** from both the active region **17** and the strap region **24**, as shown in FIGS. **3**I and **4**I. An anisotropic poly etch follows to remove the portion of poly layer **14** not covered by oxide spacers **44** and oxide layer **58** in the active region **17** (FIG. **3**J). The poly etch has no affect on the strap region **24** (FIG. **4**J). The nitride and poly etch steps effectively create second trenches **60**, one on either side of the mirror pair of memory cells in the active region **17**, as well as upwardly projecting sharp edges **62** on side edges of poly layer **14**. A controlled isotropic oxide etch is then performed, to remove exposed portions of oxide layer **12**, and to remove a small portion of spacers **44** directly over the sharp edges **62**. This oxide etch has a negligible effect on the strap region **24**. The resulting structures are shown in FIGS. **3**J and **4**J.

The next step is an oxidation process, which forms an oxide layer on the exposed ends **64** of poly layer **14** (strap region **24** unaffected). Oxide layer **64** joins with oxide layer **42** in forming an insulation layer that is disposed adjacent to and over the polysilicon layer **14**. The sharp edges **62** and the thickness of the insulation layer formed by oxide layers **64**/**42**, permit Fowler-Nordheim tunneling of charges therethrough. The oxidation process also re-forms oxide layer **12** over the exposed portions of the substrate **10**. The deposition of a thick poly layer **66** over the active region and strap region structures follows, as illustrated in FIGS. **3**K and **4**K.

While not shown in the above figures, at least one peripheral region **130** of the substrate **10** is disposed adjacent to the memory cell array. Logic devices, are formed in the peripheral region that relate to the operation of the memory cell array. For the purposes of the present invention, logic devices include low or high voltage MOS FET's, and passive elements such as capacitors or resistors. As shown starting with FIG. **3**L, the peripheral region **130** is preferably separated from one of the active regions **17** by an isolation region **132** (such as STI isolation as described above) formed in the substrate **10**. Poly layer **66** formed over the active region **17** extends over the peripheral region **130**. FIG. **4**L illustrates the same strap region **24** as shown in FIG. **4**K.

A masking step is performed, where photo resist is formed over the structure, and removed only from the peripheral region **130**, leaving photo resist **134** disposed over active region **17** and the strap region **24**, as shown in FIGS. **3**M and **4**M. A poly (anisotropic) etch process is then performed to remove the exposed portion of poly layer **66** in the peripheral region **130** (using oxide layer **12** as an etch stop). The portions of poly layer **66** protected by the photo resist **134** in the active and strap regions **17**/**24** are unaffected by the poly etch step, as shown in FIGS. **3**N and **4**N.

After the photo resist **134** is removed, a well region **136** is formed in the peripheral region **130** of substrate **10** by masking the structure except for the peripheral region **130**, and performing suitable ion implantation (i.e. well implant, punch through implant and Vt implant) through oxide layer **12** to form one or more well regions **136** as shown in FIG. **3**O. In the preferred embodiment, well region **136** is N type. A separate and similar masking step can be employed to form a p-type well. The masking material is then removed, followed by an oxide etch that removes the exposed portions of oxide layer **12** from the peripheral region **130** (using the substrate **10** as an etch stop). An oxide layer **138** is formed on the exposed surfaces of the structure. The portion of oxide layer **138** in the peripheral region **130** will form the gate oxide of the logic devices formed therein, and thus oxide layer **138** will have a thickness appropriate for the voltage requirements of such logic devices. The resulting structures in the active, peripheral and strap regions are shown in FIGS. **3**O and **4**O.

A layer of polysilicon is next deposited over the structure, following by photo resist **140** formed over the polysilicon layer. A masking step is then used to remove the photo resist **140** except for locations under which transistor (logic) gates are to be formed in the peripheral region **130**. A dry poly etch process is then used to remove the deposited poly layer except for poly spacers **142** adjacent vertical portions of oxide layer **138**, and poly blocks **144** underneath the remaining portions of photo resist **140**. Poly spacers **142** are conductive residue that should be removed to prevent electrical shorts in the device, and poly blocks **144** form the logic (transistor) gates of the logic devices formed in the peripheral region **130**. The resulting structures are shown in FIGS. **3**P and **4**P.

The remaining photo resist **140** is removed. New photo resist **146** is formed over the structure. A masking step is used to remove the photo resist **146** except for over the peripheral region **130**. A poly etch process is then used to remove any polysilicon residues, including poly spacers **142**, as shown in FIGS. **3**Q and **4**Q.

A wet oxide etch is performed to remove oxide layer **138** from the active region **17** and the strap region **24**. A poly etch (RIE) follows, which removes poly layer **66** from the active

region **17** except for poly spacers **68** next to oxide spacers **44**, as shown in FIG. **3**R. In the strap region **24**, the poly etch removes poly layer **66** except for poly spacers **70** next to oxide blocks **46**, and poly block **72** between oxide blocks **46**, as shown in FIG. **4**R. The width W" between the oxide blocks **46** needs to be small enough compared to the thickness of the deposited polysilicon **66** so that poly block **72** fills the space between oxide blocks **46** and has a planar upper surface after the poly etch process. Specifically, width W" should be no greater than approximately twice the thickness T' of the deposited polysilicon, as shown in FIGS. **4**K and **4**R.

Photo resist **146** is then removed. Nitride is deposited over the structures, followed by an anisotropic nitride etch (such as RIE dry etch) to remove all the deposited nitride except for spacers **74** adjacent poly spacers **68** in the active region **17** (FIG. **3**S), spacers **75** adjacent poly blocks **144** in the peripheral region **130** (FIG. **3**S), and spacers **76** adjacent to poly spacers **70** in the strap region **24** (FIG. **4**S). The peripheral region **130** is masked with photo resist while ion implantation (e.g. N+) is then used to form second regions (i.e. drain regions) **78** in the active region substrate in the same manner as the first regions **50** were formed. Then, the active region **17** is masked with photo resist while ion implantation (e.g. P+) is then used to form source and drain regions (third and fourth regions) **122/124** in the well region **136** in a similar manner as the first region **50** was formed, as shown in FIG. **3**S. The first and second regions **50/78** have a conductivity type (e.g. N type) that is different from that of the substrate **10**. Likewise, third and fourth regions **122/124** have a conductivity type (e.g. P type) that is different from that of the well region **136**. These ion implantations have no effect on the strap region **24**, as shown in FIG. **4**S.

A thin oxide etch is performed to remove exposed portions of oxide layers **12** and **138** over the substrate in the active and peripheral regions **17/130**, and the oxide layer **58** over poly bock **56** (no appreciable effect in strap region **24**). A metal deposition step is then performed, to deposit a metal such as tungsten, cobalt, titanium, nickel, platinum, or molybdenum over the active, peripheral and strap region structures. The structures are then annealed, permitting the hot metal to flow and to seep into the exposed top portions of the substrate **10** to form a conductive layer of metalized silicon **80** (silicide) on the substrate next to side wall spacers **74** and **75**. Metalized silicon region **80** on substrate **10** can be called self aligned silicide (i.e. salicide), because it is self aligned to the second regions **78** by spacers **74** and to third/fourth regions **122/124** by spacers **75**. The hot metal also forms a conductive layer of metalized polysilicon **82** (polycide) on the exposed top portions of poly spacers **68** (in active region **17**), poly blocks **56** (in active region **17**), poly blocks **144** (in peripheral region **130**), poly spacers **70** (in strap region **24**) and poly blocks **72** (in strap region **24**). The rest of the metal deposited on the remaining structure is removed by a metal etch process.

Passivation, such as BPSG **84**, is used to cover the structures. A masking step is performed to define etching areas over the second regions **78** (in active region **17**) and the poly blocks **72** (in strap region **24**). The BPSG **84** is selectively etched in the etching areas to create contact openings that are ideally centered over the second regions **78** and poly blocks **72**. The contact openings are then filled with conductor metal contacts **86** and **102** by metal deposition and planarizing etch-back. The salicide and polycide layers **80/82** enhance conduction between the conductors **86/102** and the second regions **78** or poly blocks **72**. In each of the active regions **17**, a bit line **88** is added by metal masking over the BPSG **84** to connect together all the contacts **86** in the active regions. In the strap region, strap jumpers **90** are added by metal masking over the BPSG **84** to connect to contacts **102**.

A metal source line strap **112** and a pair of metal word line straps **114** and **116** are formed over, and extend parallel to, each row of memory cells preferably by a similar metal masking process used to form bit lines **88**. In the strap region, a metal via **118** is formed to connect the strap jumper **90** with the appropriate strap **112/114/116**. The metal via **90** shown in FIG. **4**S connects the strap jumper **90** with the word line strap **116**. Metal straps **112/114/116**, jumpers **90** and metal via's **118** are surrounded by an appropriate insulation material **120**, such as oxide. The final active region memory cell structure is illustrated in FIG. **3**S, and the final strap region structure is illustrated in FIG. **4**S.

As shown in FIG. **3**S, first and second regions **50/78** form the source and drain for each memory cell (those skilled in the art know that source and drain can be switched during operation). The channel region **92** for each cell is the portion of the substrate that is in-between the source and drain **50/78**. Poly spacers **68** constitute the control gates, and poly layer **14** constitutes the floating gate. The control gates **68** have a lower first portion **94** that is disposed adjacent the floating gate **14** (insulated therefrom by oxide layer **64**), and an upper second portion **96** that protrudes over the sharp edge **62** of floating gate **14**. Floating gate **14** is disposed over part of the channel region **92**, is partially overlapped at one end by the control gate **68**, and partially overlaps the first region **50** with its other end. The process of the present invention forms pairs of memory cells that mirror each other, where each pair of memory cells shares a single source region **50**. The non-volatile memory cells are of the split gate type having floating gate to control gate tunneling all as described in U.S. Pat. No. 5,572,054, whose disclosure is incorporated herein by reference with regard to the operation of such a non-volatile memory cell and an array formed thereby. Also shown in FIG. **3**S are logic devices **148** formed in the peripheral region **130**. The logic devices **148** include poly gates **144** disposed over the well region **136** and insulated therefrom by the gate oxide layer **138**. The poly gates **144** selectively activate (i.e. turn on) channel regions **93** of substrate **10** disposed between third and fourth regions **122/124**. Logic devices **148** are low voltage (e.g. ~3V) or high voltage (e.g. ~12V) MOS FET's, where the thickness of the oxide layer **138** and the implantation depth and concentration of the third and fourth regions **122/124** dictate the breakdown voltage of the logic devices **148**.

Strap Regions

FIG. **4**S is the final cross sectional view of one portion of the 'H' shaped trench pattern formed strap region **24** (corresponding to line **4**B—**4**B of the mask **30** in FIG. **5**). FIGS. **6**A, **6**B and **6**C illustrate cross sections of other portions of the trench pattern formed in strap region **24**, corresponding to lines **6**A—**6**A, **6**B—**6**B and **6**C—**6**C, respectively, of mask **30** in FIG. **5**, and as shown in FIG. **7**. These figures illustrate, given the proper dimensions of mask **30**, that conductive polysilicon is generally formed on those strap region portions imaged under the opaque portions of mask region **32**, and silicon dioxide is generally formed on those strap region portions imaged under the transparent aperture portions of mask region **32**.

Thus, the final layout of the structure is illustrated in FIG. **7**. Columns of strap regions **24** are interlaced with columns of memory cell arrays **98**, where the memory cell arrays **98**

include columns of active regions **17** interlaced with columns of isolation regions **16**. Each row in each strap region **24** includes a WL strap cell **28** disposed between a pair of SL strap cells **29**, all aligned with one of the memory cell rows. The active regions **17** immediately adjacent to the WL strap cells **28** are actually dummy regions that do not contain any active memory cells, but rather are part of the strap region **24** and used to form the SL strap cells **29**.

The control gates **68** for each row of memory cells are continuously formed as a single word line **69** that connects together all the control gates **68** in that row of memory cells. Each of the word lines **69** pass through the strap regions **24**. An 'L' shaped contact lead **100** (corresponding to one of the 'L' shaped members **35** of mask **30**) extends from each of the word lines **69** toward the center of the WL strap cell **28**, and terminates with the electrical contact **102** formed thereon. Each of the word line straps **114/116** extend parallel to one of the word lines **69**, with intermittent electrical contact therebetween in the strap regions **24** by metal contacts **102**, metal jumpers **90** and metal via's **118**. The metal word line straps **114/116** ensure that a substantially even voltage is applied along the entire length of each of the word lines **69**.

The poly blocks **56** (disposed over source regions **50**) for each row of memory cells pairs are continuously formed as a single source line **57** that connects together all the poly blocks **56** (and source regions **50** connected thereto) in that row of memory cell pairs. Each of the source lines **57** terminate in the SL strap cells **29**, and do not pass through the strap regions **24**. Instead, each source line **57** terminates with an electrical contact **104** formed near the center of the SL strap cell **29** in a similar manner as the bit line contacts **86**, as shown in FIG. **7**. The metal source line straps **112** connect together the contacts **104** in the strap cells **29** through metal via **118** and metal strap jumper **90**. In the preferred embodiment, the metal source line straps **112** each extend parallel to source lines **57**, with contact to the underlying source line **57** by contacts **104** in strap cells **29**. Alternately, source line straps **112** could simply extend from one SL strap cell **29**, over or around the WL strap cell **28**, to the other SL strap cell **29** in the same strap region **24**. In any event, word line straps **114/116**, source line straps **112**, and bit lines **88** are all metal conduit that are three-dimensionally configured (lateral spacing and height above the memory cell array) in and above the BPSG so as to not interfere with each other, yet each connect between with the appropriate voltage source and strap regions with minimal space requirements.

FIG. **8** illustrates various dimensions of the strap region **24** that can be optimized to best form electrical contacts **102** and **104** without shorting the word lines **69** to each other, or to the source line **57**. W1 to W7 (and L1 to L6) are ideally set so any inadvertent horizontal (and/or vertical) shifts of any of the strap region elements would not result in an improperly formed contact or an inadvertent short. However, certain dimensions must be small enough to prevent the formation of the source line **57** in the strap region **24**. For example, for many applications, the dimensions between conductive elements (e.g. L1, L3, W2) should be no greater than approximately twice the thickness T of the insulation layer deposited to form the insulation therebetween. Thus, the deposited insulation is not removed by subsequent etch steps to prevent the formation of conductive material in these regions.

With the present invention, additional room is made within the strap regions **24** because the source lines **57** do not traverse therethrough. This additional room allows the strap cells **28** and contacts formed therewith to be formed within the "effective width" of the memory cell row, and even along the row centerlines, as opposed to extending out toward adjacent memory cell rows as shown in FIG. **1**. The "effective width" of a memory cell row is the distance (in the Y direction) taken up by the conductive memory cell components (e.g. floating gate, source line, control gate or control line, etc.) formed above the substrate. Thus, for the mirror cells illustrated in the figures, the "effective width" of each row is the distance between the two word lines **69** in each row of memory cells (distances L_4, L_5 and L_6) plus the widths of the two word lines **69** themselves. This is important because the word line electrical contacts **9***a* in FIG. **1** had to be formed outside of the effective width of the corresponding row of memory cells. As a result, the scaling down of the memory cell array along the "Y" direction was consequently prohibited because extra (wasted) space between memory cell rows was necessary to leave room for these electrical contacts. The present invention removes this constraint by allowing strap cells **28** to be formed within the effective width of the memory cell row, and in some embodiments even within the distance between pairs of word lines in each row, to form rows of memory cells in the array that are closer together (in the Y direction). Further, for any given size strap cell region **24**, the extra room allows contacts **102** to be formed further apart to reduce the risk of shorting word or source lines together. Finally, the extra room within the strap regions **24** allows them, and the memory cell array as whole, to be safely scaled down in size in both the X (row) and Y (column) directions.

It should be noted that by following the same concepts as demonstration above, other configurations of mask **30** can be used to form strap regions **24** according to the present invention. For example, FIGS. **9A**, **10A**, **11A** and **12A** are alternate embodiments of mask **30**, where the patterned aperture **31** resembles an 'S' shape (FIG. **9A**), a '$' shape (FIG. **10A**), an 'I' shape (FIG. **11A**), or a modified 'S' shape (FIG. **12A**).

The 'S' shaped mask **30** of FIG. **9A** includes a pair of tab members **106** that extend out from opposing sides of aperture **31** to form an 'S' shaped aperture. The cross-section of the resulting structure imaged under the tab members **106** is illustrated in FIG. **9B**, and the resulting layout of the final structure is illustrated in FIG. **9C**.

The '$' shaped mask **30** of FIG. **10A** is similar to that shown in FIG. **9A**, but further includes opposing tab members **108***a* and **108***b* that extend out from opposing sides of aperture **31** to form a '$' shaped aperture **31**. The cross-sections of the resulting structure imaged under the tab members **106** and under tab members **108***a*/*b* are illustrated in FIGS. **10B** and **10C** respectively, and the resulting layout of the final structure is illustrated in FIG. **10D**.

The 'I' shaped mask **30** of FIG. **11A** includes a pair of directly opposing tab members **110** that extend out from opposing sides of aperture **31** to form an 'I' shaped aperture **31**. The cross-section of the resulting structure imaged under the tab members **110** is illustrated in FIG. **11B**, and the resulting layout of the final structure is illustrated in FIG. **1C**.

The modified 'S' shaped mask **30** of FIG. **12A** includes a pair of 'L' shaped tab members **106** that are similar to the 'L' shaped tabs **35** shown in FIG. **5**. The tabs **106** extend out from opposing sides of aperture **31**, and then extend away from each other, to form an 'S' shaped aperture. The cross-section of the resulting structure imaged under the tab members **106** is illustrated in FIG. **12B**, and the resulting layout of the final structure is illustrated in FIG. **12C**.

Each of the masks shown in FIGS. **9A**, **10A**, **11A** or **12A** result in a strap region **24** which is not traversed by the source line **57**, and provides locations for forming the word line and source line contacts **102/104** that are sufficiently spaced apart from each other and from other strap region elements.

FIG. **13** shows the three-dimensional topography of the active region structure of FIG. **3P**, including the word line termination area **126** in which the source line **57** extends from the end of the row of memory cell pairs. The structure has two different levels upon which residual poly spacers **142** are formed, and need removal. Specifically, residual poly spacers **142** are formed over the substrate and over the poly layer **66** (insulated therefrom in both cases by oxide layer **138**). Removal of residual polysilicon would be easier if the topography of the structure was simplified and resulted in the formation of as few as one residual poly spacer **146** for each row of memory cell pairs. The first alternate embodiment provides such a method and structure.

First Alternate Embodiment

FIGS. **14A–14K** and **15A–15K** illustrate a first alternate embodiment for forming the logic devices in the peripheral area **130** and the associated memory cells in the active region **17**. In this embodiment, there is a reduction and simplification of the structure topography in the active region **17** earlier in the process, which minimizes the formation of unwanted residual polysilicon (i.e. poly stringers) that are formed in later process steps.

This first alternate embodiment starts with the structure shown in FIGS. **3L** and **4L** (reproduced in FIGS. **14A** and **15A**). A thick nitride layer **150** (~1500 Å) is formed over poly layer **66**, as shown in FIGS. **14B** and **15B**. The entire structure is then planarized preferably employing a chemical-mechanical polishing (CMP) process that uses oxide **58** as a polishing stopper. As shown in FIG. **14C**, the oxide spacers **44**, poly layer **66** and nitride layer **150** in the active and peripheral regions **17/130** are polished down even with oxide layer **58**, leaving nitride layer **150** covering poly layer **66** in the peripheral region **130** and partially covering poly layer **66** in active region **17**. As shown in FIG. **15C**, the oxide blocks **46**, poly layer **66** and nitride layer **150** are polished down even with each other in the strap region **24**, resulting in poly block **72** disposed between oxide blocks **46**, and nitride layer **150** partially covering poly layer **66** on either side of the oxide blocks **46**.

An oxidation process is performed to form a layer of oxide **152** on all exposed surfaces of poly layer **66** (i.e. adjacent oxide spacers **44** in the active region **17** and adjacent oxide blocks **46** in strap region **24**) and poly block **72**. A nitride etch process is used to remove all remaining portions of nitride layer **150**, as shown in FIGS. **14D** and **15D**. A dry poly etch follows to remove all exposed portions of poly layer **66** which are not protected by oxide layer **152**, leaving poly blocks **154** adjacent the oxide blocks **44** (in active region **17**) and poly blocks **156** adjacent oxide blocks **46** (in strap region **24**), as shown in FIGS. **14E** and **15E**.

A nitride layer **158** is formed over the active, peripheral and strap regions **17/130/24**. A masking step is used to protect active and strap regions **17/24** while a nitride etch is used to remove nitride layer **158** from the peripheral region **130** only (as shown in FIGS. **14F** and **15F**). Once the masking material is removed, the well region **136** is formed in the peripheral region **130** of substrate **10** by masking the structure except for the peripheral region **130**, and performing suitable ion implantation through oxide layer **12** (i.e. well implant, punch through implant and Vt implant) to form one or more well regions **136** as shown in FIG. **14F**. In the preferred embodiment, well region **136** is N type.

After the masking material is removed, an oxide etch is used to remove the exposed portion of oxide layer **12** from the peripheral region **130** (using the substrate **10** as an etch stop). The gate oxide layer **138** is then formed on the exposed surface of the substrate **10** using a thermal oxide process, with a thickness that is appropriate for the voltage requirements of the logic devices. A layer of polysilicon is next deposited over the structure, following by the photo resist **140** formed over the polysilicon layer. A masking step is then used to remove the photo resist **140** except for locations under which transistor (logic) gates are to be formed in the peripheral region **130**. A dry poly etch process is then used to remove the deposited poly layer except for residual poly spacers **142** adjacent vertical portions of nitride layer **158**, and poly blocks **144** underneath the remaining portions of photo resist **140**. Residual poly spacers **142** should be removed to prevent electrical shorts in the device, and poly blocks **144** form the logic (transistor) gates of the logic devices formed in the peripheral region **130**. The resulting structures are shown in FIGS. **14G** and **15G**.

The remaining photo resist **140** is removed. New photo resist **146** is formed over the structure. A masking step is used to remove the photo resist **146** except for over the peripheral region **130**. A poly etch process is then used to remove any polysilicon residue, including residual poly spacers **142**, as shown in FIGS. **14H** and **15H**. Oxide and poly etches are performed to clean oxide on the wordline **69** and disconnect the top and bottom of the wordlines in the termination area at the end of the memory cell pair row (not shown). After photo resist **146** is removed, a nitride etch process is performed to remove nitride layer **158**, as illustrated in FIGS. **141** and **151**. A thermal oxidation step follows to form oxide layer **160** on any exposed portions of poly blocks **154/144/156**, which encapsulates these poly blocks. The resulting structures are shown in FIGS. **14J** and **15J**.

The active and strap regions **17/24** are masked with photo resist while ion implantation (e.g. P+) is used to form the third and fourth regions **122/124** in the well region **136**, as shown in FIG. **14K**. Nitride is then deposited over the structures, followed by an anisotropic nitride etch (such as RIE dry etch) to remove all the deposited nitride except for spacers **162** formed against vertical portions of oxide layer **160**, which are adjacent poly blocks **154** (in the active region **17**), poly blocks **144** (in the peripheral region **130**), and poly blocks **156** (in the strap region **24**). The peripheral region **130** is then masked with photo resist while ion implantation (e.g. N+) is then used to form the second regions (i.e. drain regions) **78** in the active region substrate, as shown in FIG. **14K**.

A thin anisotropic oxide etch is performed to remove exposed portions of oxide layers **12** and **138** over the substrate **10** in the active and peripheral regions **17/130**. This oxide etch also removes the oxide layers **152/58** disposed over poly blocks **154/56/156/72**, as well as portions of oxide layer **160** disposed over poly blocks **144**. The metal deposition step is then performed, to deposit a metal (e.g. tungsten, cobalt, titanium, nickel, platinum, or molybdenum) over the active, peripheral and strap region structures. The structures are then annealed, permitting the hot metal to flow and to seep into the exposed top portions of the substrate **10** to form the salicide **80** on the substrate next to side wall spacers **162**, and into the exposed top portions of poly blocks **154/56** (in active region **17**), poly blocks **144** (in peripheral region **130**), and poly blocks

156/72 (in strap region 24) to form the layer of polycide 82 thereon. A metal etch process is used to remove the metal deposited on the remaining structure.

The remaining processing steps disclosed above with respect to FIGS. 3S and 4S (including forming BPSG 84, metal contacts 86 and 102, bit line 88, strap jumper 90, metal source line strap 112, metal word line straps 114/116, and metal via 118) are performed to result in the structures shown in FIGS. 14K and 15K. The advantages of this method and the memory cell array formed thereby are that the structure has a simplified (single level) topography such that residual polysilicon used in forming the logic device gate poly's is easier to remove, the control gates 154 have a vertically oriented back wall to more easily form insulation spacers 162, and the logic device gate poly's are formed separately from memory cell control gate poly's so that their respective thicknesses are decoupled and can be optimized separately.

FIG. 16 shows the three-dimensional topography of the active region structure of FIG. 14G, including the word line termination area 126 in which the source line 57 extends from the end of the row of memory cell pairs. This process reduces and simplifies the structure topography (i.e. resulting structure only has a single level topography upon which residual poly spacers 142 are formed), which minimizes the amount of residual polysilicon that will need removal. The resulting poly spacers 142 are fewer and smaller. In contrast, the previous embodiment as a more complicated, two level topography (see FIG. 13), which results in a much greater amount of residual polysilicon that is more difficult to remove. Electrical shorts can occur in devices with residual poly stringers that were not adequately removed. The simplified topography and the reduced amount of residual polysilicon in the present embodiment results from two key features of the method process: 1) forming the polysilicon control gates 154 before the formation of the poly gates 144 of the logic devices 148, and 2) forming the polysilicon control gates 154 before the formation of the protective layer of nitride 158 (which allows for the safe removal of the residual polysilicon). The protective layer 158 allows for the use of a thorough anisotropic poly etch for removing the poly stringers without adversely affecting the rest of the memory cell structure.

Second Alternate Embodiment

FIGS. 17A–17H and 18A–18H illustrate a second alternate embodiment for forming the logic devices in the peripheral area 130 and the associated memory cells in the active region 17. This embodiment also reduces and simplifies the structure topography in the active region earlier in the process, which minimizes the formation of unwanted residual polysilicon (i.e. poly stringers) that are formed in later process steps.

This second alternate embodiment starts with the same structure shown in FIGS. 3L and 4L (reproduced in FIGS. 14A and 15A), as shown in FIGS. 17A and 18A. A poly etch (RIE) is performed to remove poly layer 66 from the active region 17 except for the poly spacers 68 next to oxide spacers 44, as shown in FIG. 17B. In the strap region 24, the poly etch removes poly layer 66 except for the poly spacers 70 next to oxide blocks 46, and the poly block 72 between oxide blocks 46, as shown in FIG. 18B. As with the first embodiment, the width W" between the oxide blocks 46 needs to be small enough (e.g. no greater than approximately twice the thickness T' of the deposited polysilicon) so that poly block 72 fills the space between oxide blocks 46.

Nitride layer 158 is formed over the active, peripheral and strap regions 17/130/24. A masking step is used to protect active and strap regions 17/24 while a nitride etch is used to remove nitride layer 158 from the peripheral region 130 only (as shown in FIGS. 17C and 18C). Once the masking material is removed, the well region 136 is formed in the peripheral region 130 of substrate 10 by masking the structure except for a designated area in the peripheral region 130, and performing suitable ion implantation through oxide layer 12 (i.e. well implant, punch through implant and Vt implant) to form one or more well regions 136 as shown in FIG. 17C. In the preferred embodiment, well region 136 is N type.

An oxide etch is used to remove the exposed portion of oxide layer 12 from the peripheral region 130 (using the substrate 10 as an etch stop). The gate oxide layer 138 is formed on the exposed surface of the substrate 10 using a thermal oxide process, and thus will have a thickness appropriate for the voltage requirements of the logic devices. A layer of polysilicon is next deposited over the structure, following by the photo resist 140 formed over the polysilicon layer. A masking step is then used to remove the photo resist 140 except for locations under which transistor (logic) gates are to be formed in the peripheral region 130. A dry poly etch process is then used to remove the deposited poly layer except for residual poly spacers 142 adjacent vertical portions of nitride layer 158, and poly blocks 144 underneath the remaining portions of photo resist 140, as illustrated in FIGS. 17D and 18D.

The remaining photo resist 140 is removed. New photo resist 146 is formed over the structure. A masking step is used to remove the photo resist 146 except for over the peripheral region 130. A poly etch process is then used to remove any polysilicon residue, including residual poly spacers 142, as shown in FIGS. 17E and 18E. Oxide and poly etches are performed to clean oxide on the wordline 69 and disconnect the top and bottom of the wordlines in the termination area at the end of the memory cell pair row (not shown). After photo resist 146 is removed, a nitride etch process is performed to remove nitride layer 158, as illustrated in FIGS. 17F and 18F. A thermal oxidation step follows to form oxide layer 160 on exposed portions of polysilicon (i.e. poly spacers 68 and 70, and poly blocks 72/144), which encapsulates these poly spacers/blocks. The resulting structures are shown in FIGS. 17G and 18G.

The active and strap regions 17/24 are masked with photo resist while ion implantation (e.g. P+) is used to form the third and fourth regions 122/124 in the well region 136, as shown in FIG. 17H. Nitride is then deposited over the structures, followed by an anisotropic nitride etch (such as RIE dry etch) to remove all the deposited nitride except for spacers 162 formed against oxide layers 160, which are adjacent poly spacers 68 (in the active region 17), poly blocks 144 (in the peripheral region 130), and poly spacers 70 (in the strap region 24). The peripheral region 130 is then masked with photo resist while ion implantation (e.g. N+) is then used to form the second regions (i.e. drain regions) 78 in the active region substrate, as shown in FIG. 17H. The same implant can be optionally used to form the source and drain regions for N-type MOSFETs (not shown) as is well known in the art.

A thin anisotropic oxide etch is performed to remove exposed portions of oxide layers 12 and 138 over the substrate 10 in the active and peripheral regions 17/130. This oxide etch also removes the portions of oxide layer 160 disposed over poly spacers/blocks 68/56/144/70/72. The metal deposition step is then performed, to deposit a metal (e.g. tungsten, cobalt, titanium, nickel, platinum, or molybdenum) over the active, peripheral and strap region

structures. The structures are then annealed, permitting the hot metal to flow and to seep into the exposed top portions of the substrate **10** to form the salicide **80** on the substrate next to side wall spacers **162**, and into the exposed top portions of poly spacers/blocks **68/56/144/70/72** to form the layer of polycide **82** thereon. A metal etch process is used to remove the metal deposited on the remaining structure.

The remaining processing steps disclosed above with respect to FIGS. **3**S and **4**S (including forming BPSG **84**, metal contacts **86** and **102**, bit line **88**, strap jumpers **90**, metal source line strap **112**, metal word line straps **114/116**, and metal via **118**) are performed to result in the structures shown in FIGS. **17**H and **18**H.

This process too reduces and simplifies the structure topography, and minimizes the amount of residual polysilicon that will need removal, in the same manner as described above with respect to the first alternate embodiment. Namely, the polysilicon control gates **154** are formed before the formation of the poly gates **144** of the logic devices **148**, and before the formation of the protective layer of nitride **158**.

It is to be understood that the present invention is not limited to the embodiments described above and illustrated herein, but encompasses any and all variations falling within the scope of the appended claims. For example, although the foregoing method describes the use of appropriately doped polysilicon as the conductive material used to form the memory cells and conductive word/source lines, it should be clear to those having ordinary skill in the art that any appropriate conductive material can be used. Therefore, as used in the claims, the term "conductive material" encompasses all such conductive materials (e.g. polysilicon, polysilicide, salicide, etc). In addition, any appropriate insulator can be used in place of silicon dioxide or silicon nitride. Moreover, any appropriate material whose etch property differs from silicon dioxide (or any insulator) and from polysilicon (or any conductor) can be used in place of silicon nitride. Further, as is apparent from the claims, not all method steps need be performed in the exact order illustrated or presented in the claims, but rather in any order that allows the proper formation of the memory cell of the present invention. Moreover, the masks shown and described herein are used in a positive masking step processes, where the material under the photo resist exposed to light via the patterned mask aperture **31** is eventually removed. However, negative photo resist processes are known and usable with the present invention, where the material under the photo resist not exposed to light via the patterned mask aperture is eventually removed. With such negative photo resist processes, the masks are reversed, where the opaque mask material replaces the transparent apertures, and vice versa. The word and source lines need not have a continuous width or shape, need not be straight, and need not be formed as spacers, but rather can have any size and shape that effectively connects to each memory cell or memory cell pair in the appropriate memory cell row. Source and drain regions, and/or source and bit lines, can be swapped. Finally, the strap cell method and design of the present invention is applicable to any type or design of memory cell array having lines of polysilicon extending along and connected to rows or columns of memory cells.

What is claimed is:

1. A method of making a memory device, comprising the steps of:

forming a plurality of memory cells in a memory portion of a semiconductor substrate, wherein the formation of each of the memory cells includes the steps of:

forming a floating gate of conductive material disposed over and insulated from the memory portion of the substrate, and

forming a control gate of conductive material disposed over and insulated from the memory portion of the substrate;

forming a layer of protective material over the control gates;

forming a plurality of logic devices in a peripheral region of the semiconductor substrate after the formation of the protective material layer, wherein the formation of each of the logic devices includes the step of forming a block of conductive material disposed over and insulated from the peripheral region of the substrate, and wherein the formation of the blocks of conductive material includes the formation of residual conductive material on the layer of protective material; and

removing the residual conductive material without removing the conductive material of the control gates.

2. The method of claim **1**, wherein the formation of each of the memory cells further includes forming spaced apart first and second regions in the memory portion of the substrate having a conductivity type different from that of a portion of the substrate adjacent thereto, with a first channel region of the substrate defined therebetween, wherein at least a portion of the floating gate and at least a portion of the control gate are disposed over and insulated from the first channel region of the substrate.

3. The method of claim **2**, wherein the formation of each of the logic devices further includes forming spaced apart third and fourth regions in the peripheral region of the substrate having a conductivity type different from that of a portion of the substrate adjacent thereto, with a second channel region of the substrate defined therebetween, wherein the block of conductive material is disposed over and insulated from the second channel region.

4. The method of claim **1**, wherein for each of the memory cells, the formation of the control gate further includes forming a first portion of the control gate that is laterally adjacent to and insulated from the floating gate.

5. The method of claim **4**, wherein for each of the memory cells, the formation of the control gate further includes forming a second portion of the control gate that is vertically disposed over and insulated from the floating gate.

6. The method of claim **1**, wherein the formation of the protective material layer over the control gates includes:

forming the protective material layer over both the memory and peripheral portions of the substrate, and

removing a portion of the protective material layer formed over the peripheral portion of the substrate.

7. The method of claim **1**, wherein for each of the memory cells, the protective material layer includes a vertical portion that extends up and over the control gate.

8. The method of claim **7**, wherein for each of the memory cells, the residual conductive material is formed laterally adjacent to the vertical portion of the protective material layer.

9. The method of claim **8**, wherein for each of the memory cells, the residual conductive material is formed as a spacer of the conductive material.

10. The method of claim **1**, wherein for each of the memory cells, the control gate is formed as a spacer of the conductive material.

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